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13. ABSTRACT (Maximum 200 words) The UCLA group headed by Dr.Elliott Brown and the Rockwell Scientific group headed by Dr. Michael Shaw conducted extensive research for the DARPA HERETIC Program on the integration of two heat-removal approaches with power electronic devices, (1) micro heatpipes and (2) micro spray nozzles. Two types of power devices were investigated: (1) insulated-gated bipolar transistors (IGBTs), and (2) laterally-diffused (LD) MOSFETs. Heat pipes were found to provide little or no advantage over conventional copper-based heat spreaders in both device applications. But spray nozzles made by micromachining were found to improve the heat removal of both device types through three key innovations: (1) careful design of the micronozzle to provide jets ***directly on the heat generating areas of the devices***, (2) the use of water for the spraying to take advantage of its combination of high thermal conductivity and high latent heat of vaporization, and (3) coating the top surface of the devices prior to spraying with a conformal dielectric (Parylene C) to prevent shorting by the water. Once the spray nozzles were successfully combined with the power devices, the integrated packages were used in two system demonstrations: (1) the IGBTs in an all-solid-state motor drive, and (2) the LD-MOSFETs in a 60-W (base-station grade) RF power amplifier. Each is described below:
(1) Solid-State Motor Drive. Our conventionally machined steel nozzle provided a low-pressure water spray cooling of the IGBT surfaces within a solid-state motor drive operating under speed control of a motor load. Significant challenges included the packaging of a nozzle array design in a high-power module (> 650 W dissipation) that operated with high standoff voltages (V_{rms} ~ 325 VAC). Electrical protection of the devices was achieved by a (3 micron-thick) Parylene coating. A device (IGBT) junction-to-case thermal resistance of ~ 0.007 C/W was achieved through the direct water spray cooling. (2) RF Power Amplifier. Here a bulk-micromachined spray nozzle was used to cool an LD-MOSFET transistor in a 500 MHz RF power amplifier. With the amplifier running in Class A, spray cooling at the rate of 0.14 liter/min increased the output power from 66 to 84 W and the power-added efficiency increased from 26 to 34%, all at 34-W input. In Class AB the increase in output power and power-added efficiency were less, ≈ 8%, but we found that the amplifier could be driven much harder before failure occurred. The maximum output in class AB was 79 W compared to 70 W without spraying.

14. SUBJECT TERMS
Spray cooling, heatpipes, insulated gate bipolar transistors, laterally diffused MOSFETs, solid state motor drive, RF power amplifier

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Final Report: Modular Micromachined Si Heat Removal (MOMS Heat Removal): Tasks 5 and 6: Electronic Integration and System Test

Part I: UCLA Effort

A. Introduction

RF power transistors present an interesting challenge in terms of thermal management because of their high heat flux - typically >> 1 kW/cm^2 just below the active region. This is in contrast to power electronic (60-Hz) switches that generate high absolute power but much lower heat flux. In these RF Solid State Power Amplifiers (SSPAs), thermal spreading from the active area into the chip is usually the dominant thermal-resistance mechanism, causing the devices to run at a high junction temperature, which can degrade the RF performance and reliability.

The Heat Removal by Thermo-Integrated Circuits (HERETIC) project sponsored by DARPA seeks to find innovative solutions for optimizing the thermal budget of these transistors and thus extending the range of operation for existing devices and/or maximizing power and power added efficiency at the output. The focus of this project is to study the impact of MEMS heat-removal "devices," such as microfluidic jets, that can be integrated with Si transistors.

This spray cooling technology is advantageous with some liquids, namely water, because of its highly nonlinear heat flux characteristics in temperature ranges equivalent to the thermal breakdowns for Si transistors, roughly >150 °C. This characteristic is the result of a latent heat of vaporization that occurs during the liquid's phase change into gas upon contact with the device's surface. This phenomenon should outdo conventional

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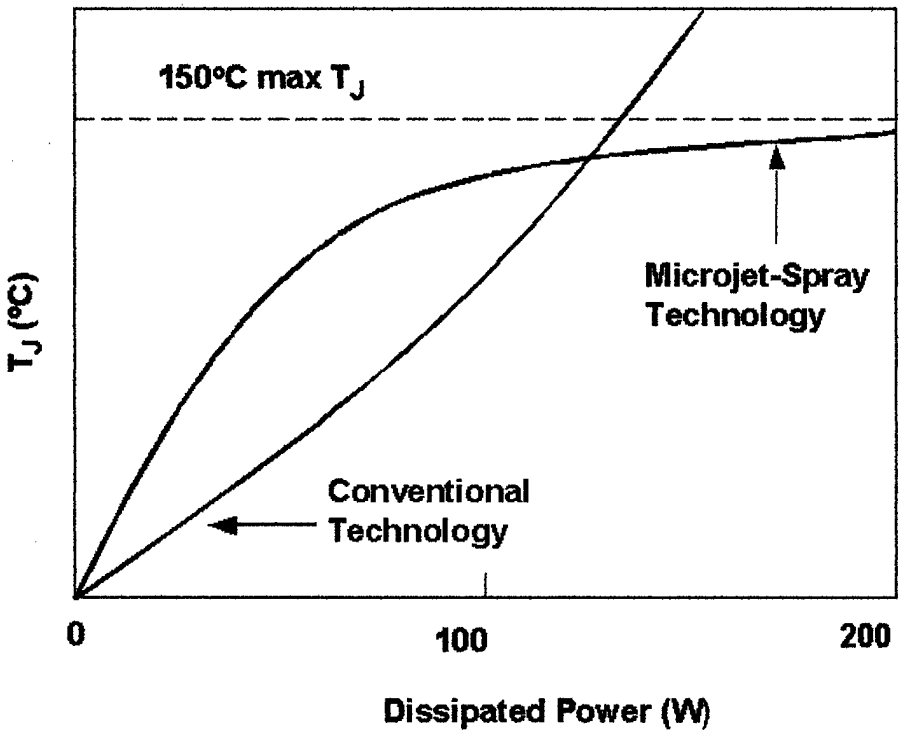

Fig. 1.

heat spreading technology for power transistors by keeping the junction temperature of power transistors below their breakdown temperature as seen in Figure 1.

B. Large-Signal Electrothermal Modeling

The modeling tool used in this project is Saber, a SPICE-like nonlinear-circuit simulator that, although very accurate, has not been used widely by the power amplifier community because of convergence problems.[1] Saber is a useful tool here because it shows effects seen more clearly in the time domain such as rise times on start up and behavior prior to reaching steady state. Saber also allows for manipulation of a thermal circuit. In the HERETIC project, this is ideal for modeling thermal conditions such as those brought about by packaging and cooling. The SSPA model that was used in these

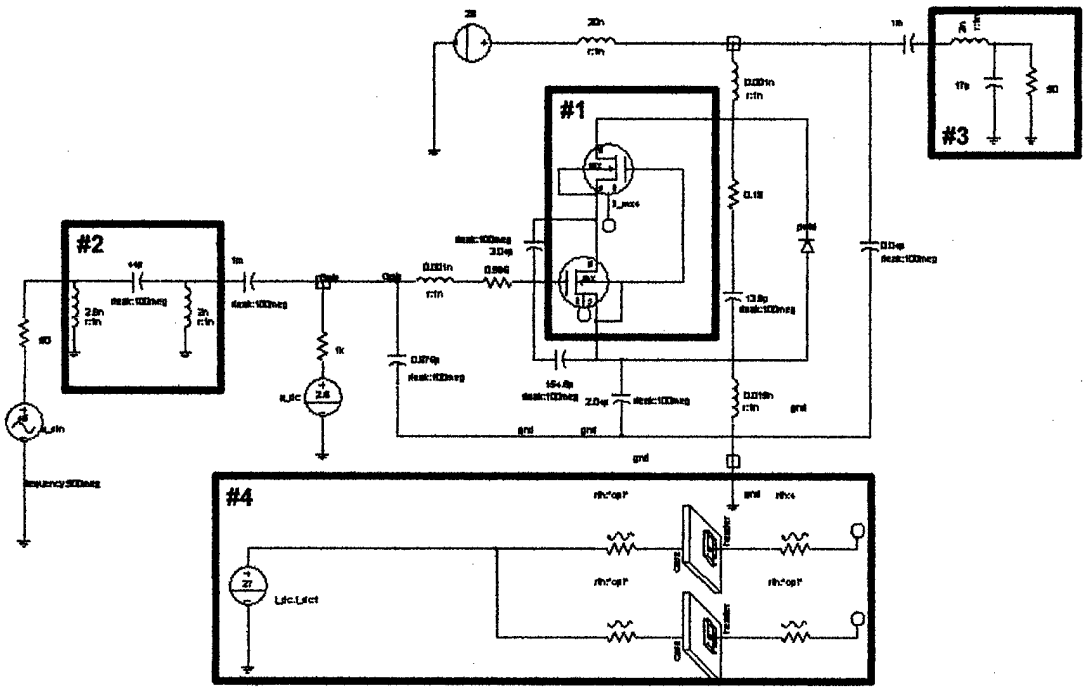

Fig. 2

experiments can be seen in Figure 2, and will be explained in groups according to the boxes marked 1,2, 3, and 4, which enclose the various circuit elements.

First, the enclosed box marked #1 represents the LDMOS device being simulated, a Polyfet LX401 65W SSPA in this case. The model shown here (based on a model provided by Polyfet RF devices[iv].) consists of two MOSFETs. The gate of the bottom most FET acts as the gate of the LDMOS device, and the source represents the source of the overall device. The body of this same FET is used to modulate the gate of the upper FET, whose drain acts as the drain for the overall device. The physical properties of each device used in the saber model are listed in Table 1. In order to match our simulated device to the actual device being modeled, IV curves were taken in saber, and device characteristics were varied to match this as closely as possible to the IV curves of the

actual device. A comparison of real and simulated IV curves can be seen in Figures 3(a) and (b).

Table 2. Saber Device Model		
	Bottom FET	Top FET
Type	n-channel	n-channel
Saber model level	1	1
V_{to} (turn on voltage)	-6.8	2.1
K_p (transconductance)	100	$0.9e^{-5}$
Lambda (channel-length modulation)	0.1	0.043
R_d (drain resistance)	0	0.06
R_s (source resistance)	0	0.07

(all omitted model values are left at their Saber defaults)

The capacitors and inductors arranged in between box 1, and boxes 2 and 3 (in Figure 2) are used to model effects of the device packaging in the frequency range of 500MHz being used, and also as chokes and blocks to keep the AC and DC signals separate, and biasing the device as necessary. The uppermost RF choke inductor (in line with the 28V DC source), which is currently set at 20nH, is also used to set the time constant which describes the turn on time of the device. For the device simulated here, the rise time to reach full power is approximately 19 ns, and the time to reach steady state is approximately 55ns. The Saber waveform showing these times is seen in Figure 5.

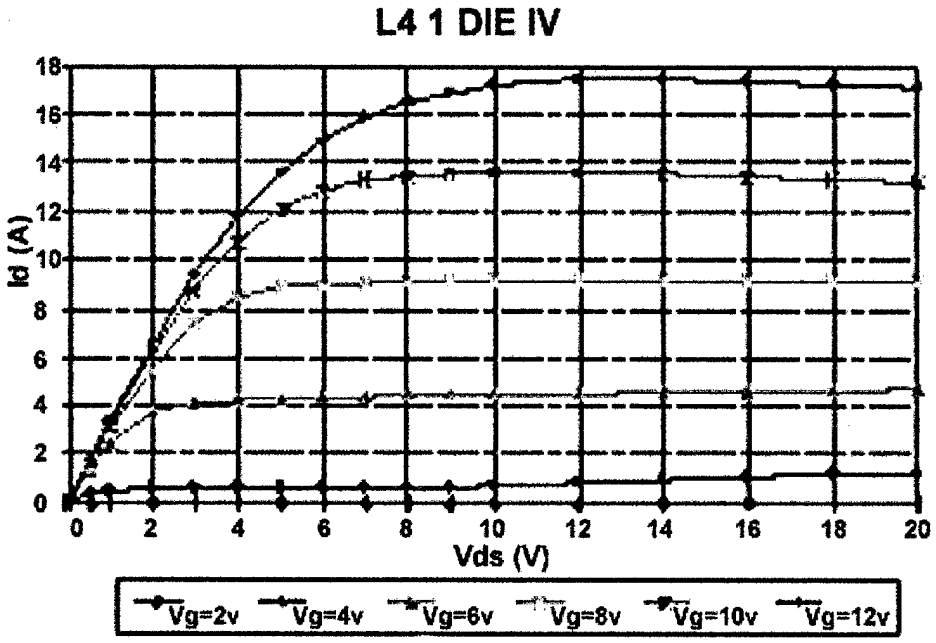
L4 1 DIE IV
Id (A)
Vds (V)
Vg=2v
Vg=4v
Vg=6v
Vg=8v
Vg=10v
Vg=12v

Fig. 3(a)

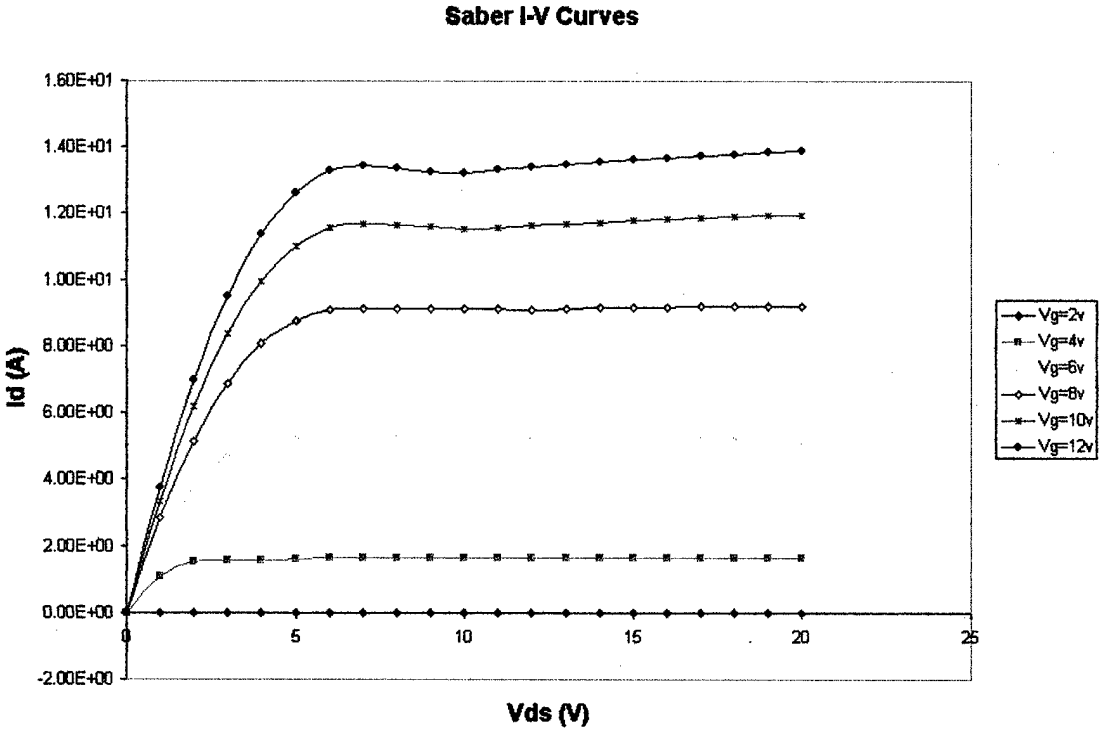
Saber I-V Curves
Id (A)
Vds (V)
Vg=2v
Vg=4v
Vg=6v
Vg=8v
Vg=10v
Vg=12v

Fig. 3(b)

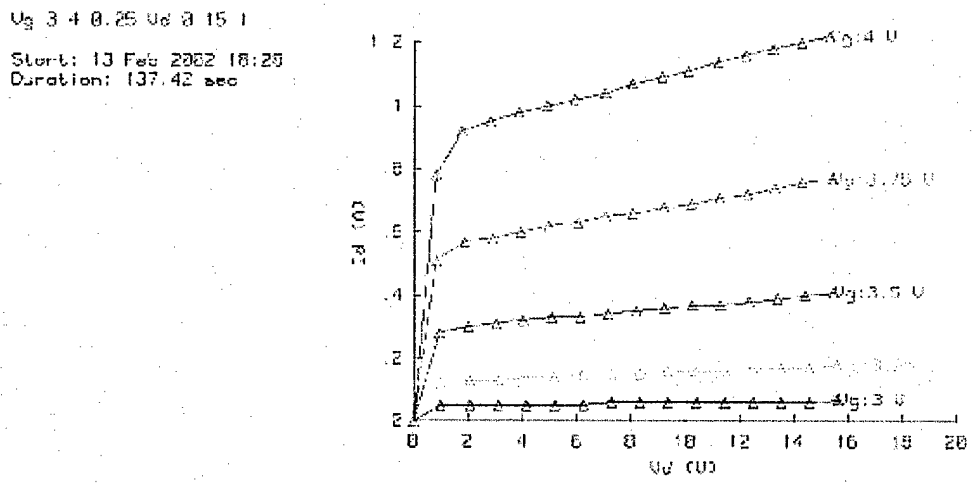
Vg 3 4 0.25 Vd 0 15 1
Start: 13 Feb 2002 18:25
Duration: 137.42 sec
Vg:4 V
Vg:3.5 V
Vg:3 V
0
2
4
6
8
10
12
14
16
18
20

Fig. 4(a)

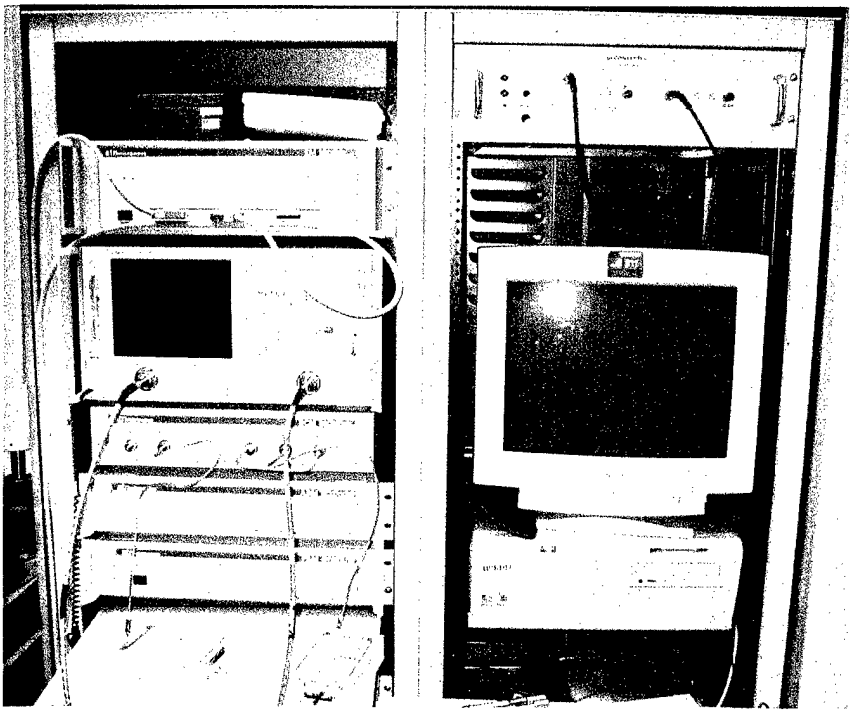

Fig. 4(b)

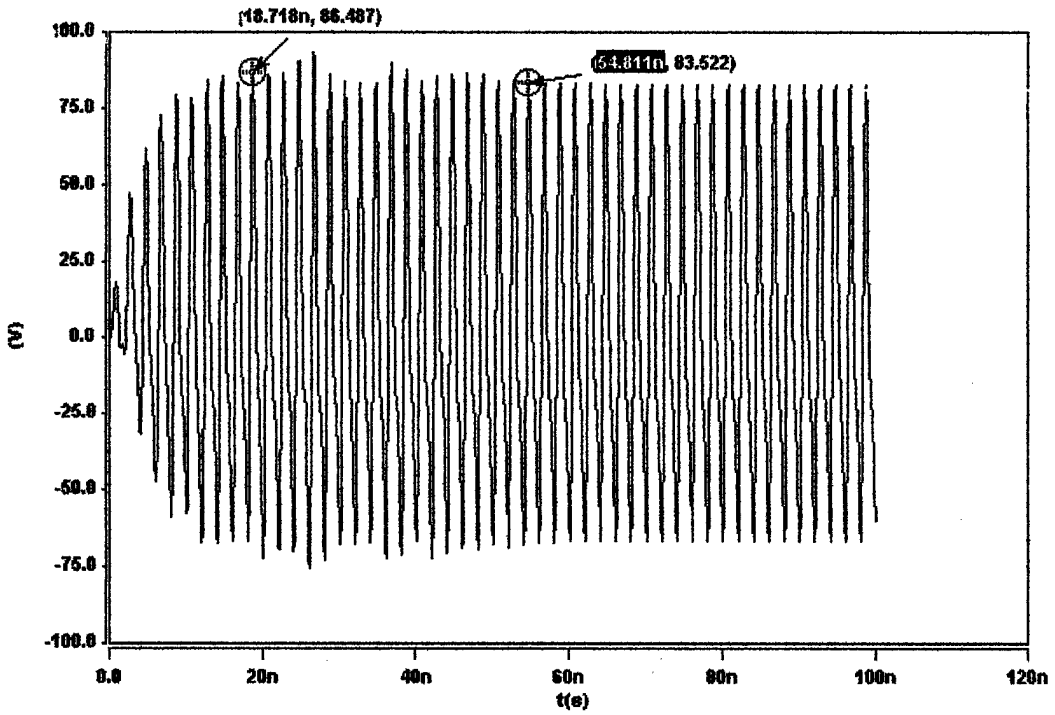

Fig. 5.

Now we will look at the enclosed box marked #2. This box encloses the input matching circuit. This is a Pi circuit, and it is being used to transform the input impedance of the device to the 50 ohms present at the output of the signal generator. A Pi circuit was chosen here because it provides enough variables to both match to 50 Ω, and provide a maximized power at the gate of the device. If the device is properly matched, a voltage divider will be seen between the 50 Ωresistances at the generator and the pi network. A Saber waveform showing this information is seen in figure 6. Figure six shows a voltage waveform across the 50 Ωresistances seen at the generator. This wave form shows an amplitude of 35 V, or little more than half of the 65 V input signal.

In order to further provide reassurance of a maximized match, an optimization loop was set up in saber which allows the individual matching circuit elements to be varied over a specified range. Saber allows the user to graph the output wave forms generated by these variations as a function of voltage. The user specifies which circuit

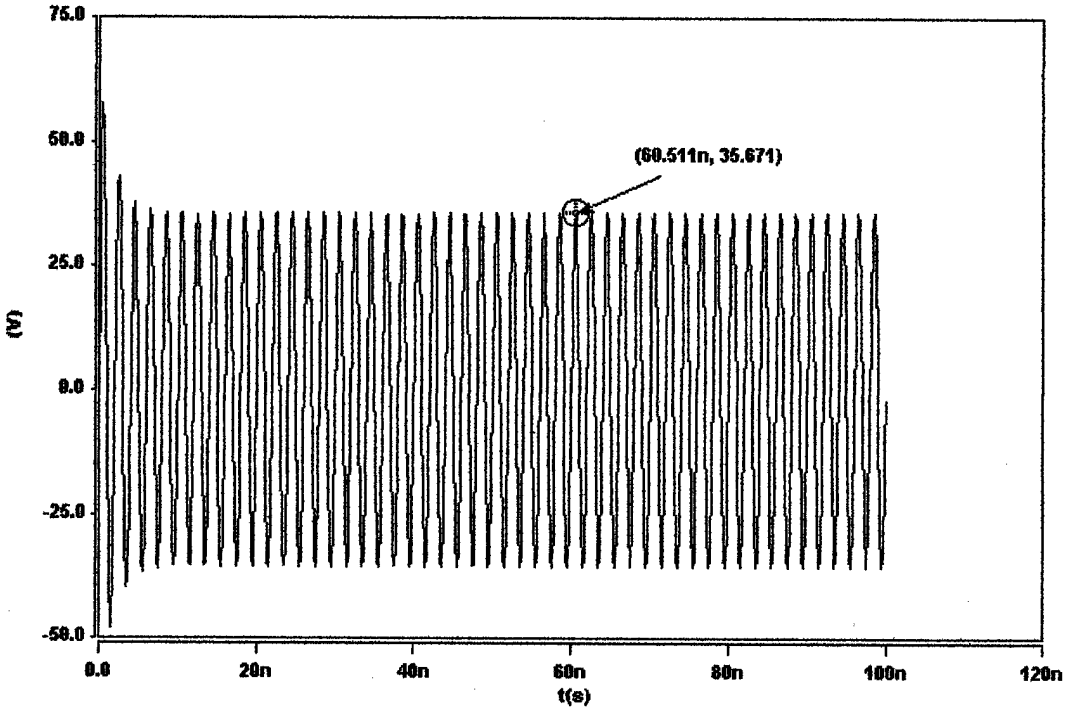

Fig. 6.

node to graph, and in this case the output of the device was chosen. From these graphs, an approach similar to that of a load-pull can be used to determine which matching circuit values should be used. Peaks in power and efficiency indicate when a proper match has been achieved.

Once an initial complex impedance for transformation is calculated, using Kerchoff's voltage and current laws arrives at device values. From here, optimization loops are once again run in saber. Resulting waveforms of inductance and capacitance vs. voltage can be seen in figures 7 (a) and (b). These waveforms are used to find the maximum in power and/or power added efficiency at the RF output load. Once all the matching circuits have been maximized for power and efficiency, the resulting saber graphs of power into the device vs. power out (figure 8) can later be compared to the actual device being tested for accuracy.

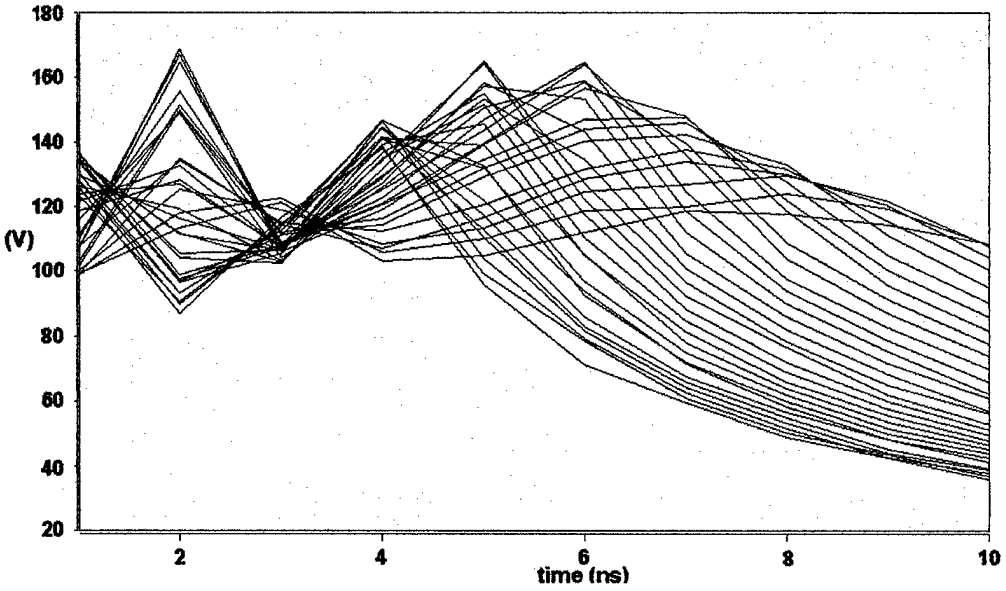

Fig. 7(a)

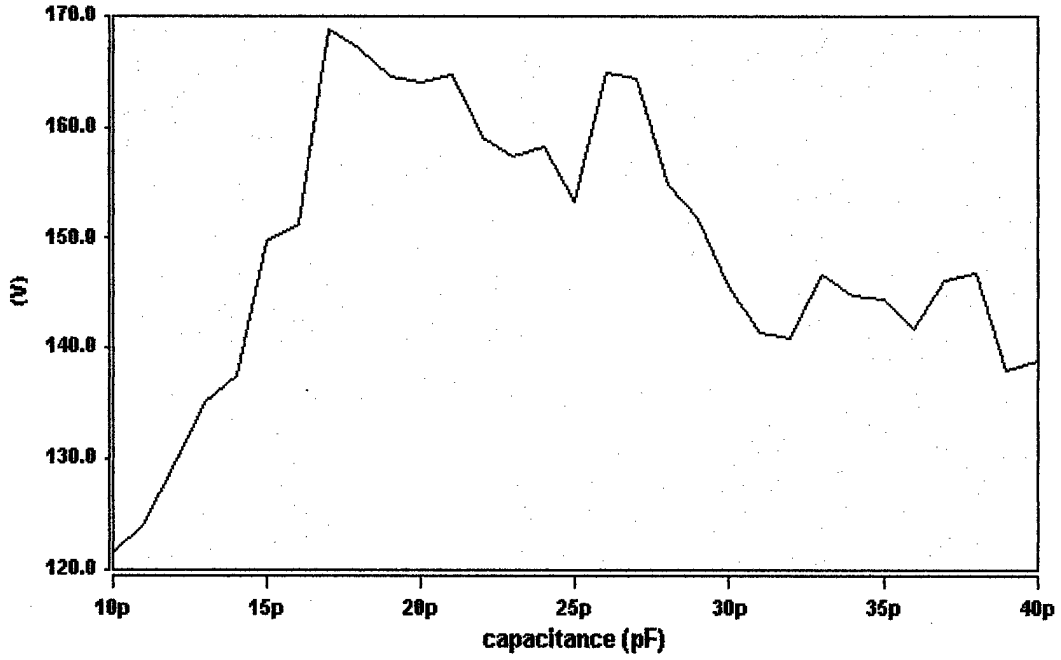

Fig. 7(b)

The next part of the simulation circuit to be explained is the enclosed box marked #3. This section represents the output matching circuit. The circuit chosen here is a low

pass LC filter. This configuration was chosen for its ability to shunt higher order harmonics through the capacitor to ground, while allowing the desired signal to pass through. In order to allow for the maximum power to be present at the 50 ohm output load, another optimization loop was constructed in Saber. This time, initial values were arrived at using criterion presented by Steve C. Cripps in his book, "RF Power Amplifiers for Wireless Communications."[2] He outlines a formula for an optimum real loadline match resistance R_{opt}, where $R_{opt} = (V_{dc} - V_{knee})^2 / 2P_{out}$. V_{dc} is the rail voltage present on the device (28 V in this case), V_{knee} is the knee voltage of the device (5 V in this case), and P_{out} is the expected output power to which the R_{opt} will be matching. Once this real impedance value is arrived at, the imaginary part of the output match must be considered as well. The imaginary part for consideration in this case is the conjugate of that which is present at the device output.

Figure 7(a) provides information on the capacitance and inductance pair that provides the maximum voltage at the output. Each of the separate lines represents one of the capacitance values simulated as a function of inductance and voltage. Figure 7(b) is the waveform that results from searching 7(a) for a maximum. It allows the user to choose the capacitance value that produces the desired output voltage, which can then be plugged back into figure 7(a) to find the inductance, which corresponds to the same output. In the case shown here, at a 10 W input and 70 W output, the graphs show that a maximum in power is arrived at with values of 2nH and 17pF.

The final enclosure on the circuit schematic is that of the thermal circuit. Saber provides certain devices with thermal nodes which can take specified information on temperature such as ambient (as seen in 27V thermal source), and packaging thermal

resistance such as that demonstrated by heat sinks located on the device, and temperature spreading effects of the solid state packaging. This thermal circuit also allows for non-linear user defined thermal resistances that can help to simulate the cooling effects in which the basis of this project is rooted. Saber waveforms of junction temperatures vs. time can be seen in Figure 8. The figure shows the junction temperature versus time for the bottom most FET in the circuit model. This simulation was run at an input power of 11W, and an output power of 71W, about 5 W above the suggested maximum of the device. The graph clearly demonstrates the non-linearity of the temperature at start up, which eventually settles (after about 55 ns) to steady state, and a temperature of 141 °C.

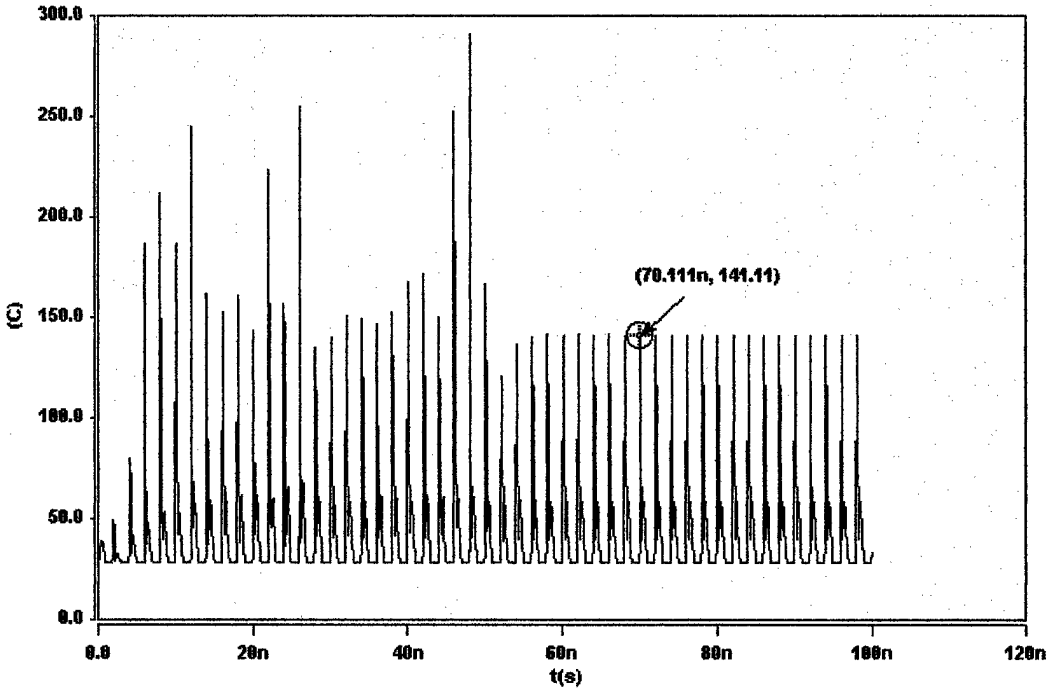

Fig. 8

C. Construction and packaging of the LX401

In order to test the LX401, it was packaged in a focus microwave PJT-1-APC7 test fixture. The fixture consists of one fixed, and one movable, plated aluminum block; both of which act as an RF ground plane. The two halves of the fixture are mounted on a flat; metal base with four adjustable legs. On top of each block, a duroid substrate with 50 Ω gold microstrip line is mounted. The SSPA to be tested is mounted on the microstrip where the two blocks meet. The source of the device sits on a copper insert, between the two blocks, which directly grounds the source. The gate and drain are held firmly against the microstrip line by way of a teflon transistor clamp, or in the case of this experiment, by soldering directly. The fixture comes with APC 7 connectors, and is rated for use up to 100W. Test fixture specifications can be seen in table 2. The test fixture itself can be seen in Figure 9.

PJT-1 Test Fixture Specifications	
Frequency Range	0 – 18 GHz
Return Loss	> 20dB
Insertion Loss	< 0.5dB
Connectors	APC-7
Power Dissipation	100W
Size	5.25 x 2.0 x 3.12"
Weight	1.5 kg
Material	Plated Aluminum
Transistor Clamp	Teflon

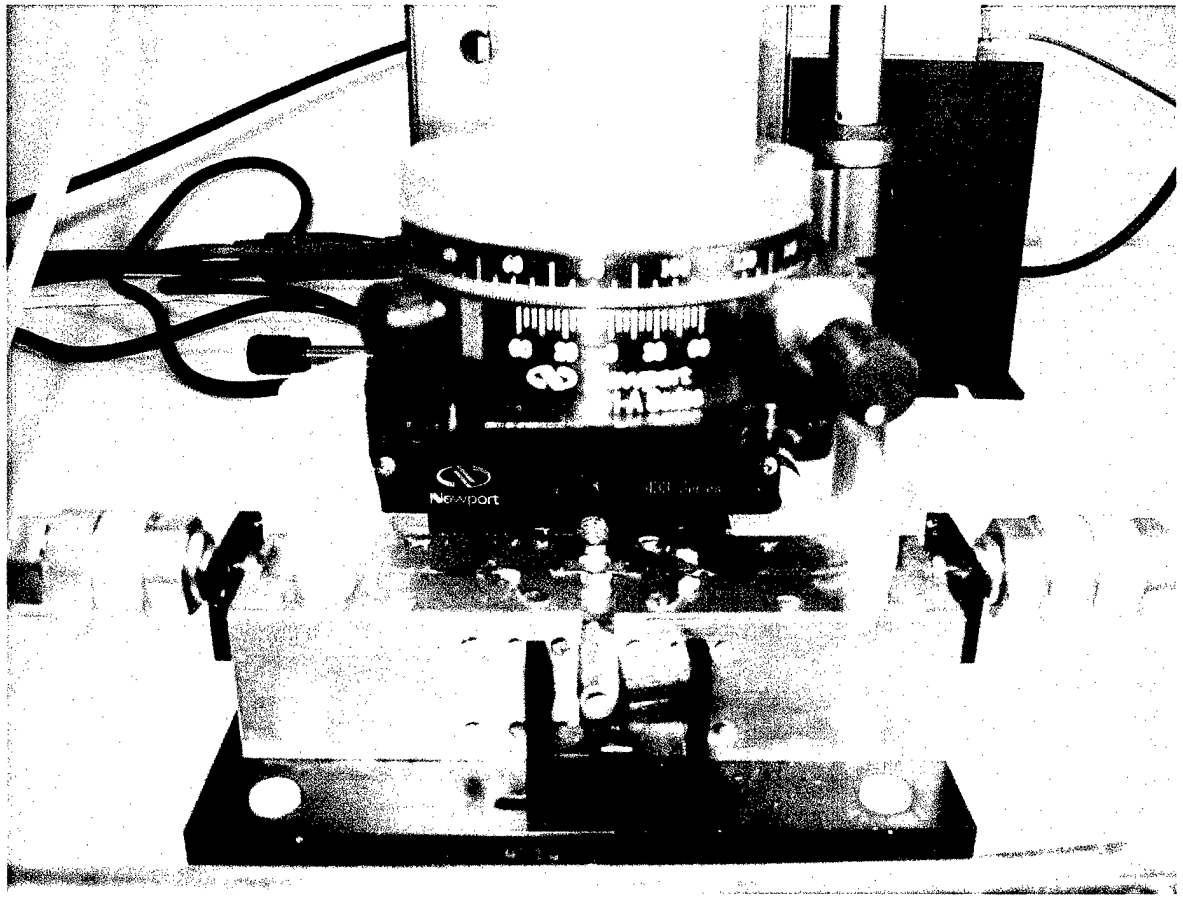

Fig. 9.

The next part of the test configuration for consideration is the biasing network. The DC biasing is separated from the RF signal by using two pico-second bias tees, connected to the gate and drain of the device. These tees are rated at 7 amps and 100 volts. Two dc power supplies (HP 6205B, and HP 6267B) are used to bias the gate between 2 and 4 V, and the drain at 28 V. The RF signal is generated at a frequency of 500 MHz by an HP 8657A signal generator. In order to attain powers upwards of 20 W at the device input, a mini-circuits LZY-1 amplifier is used. At the RF output of the device, a 27 dB RF attenuator is used to bring the signal back down to levels usable by

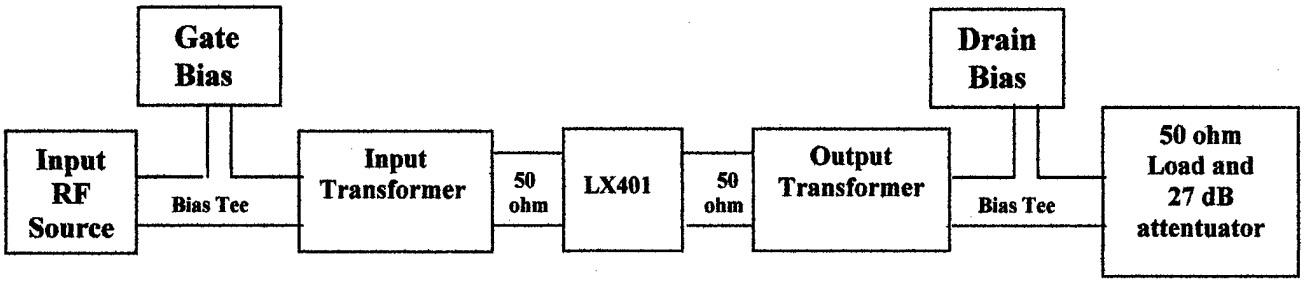

Fig. 10

block diagram of the test setup can be seen in Figure 10.

As in every RF power amplifier, a key issue in the design is large-signal impedance matching, which depends critically on transistor characteristics. To achieve the maximum gain and Pout from the device, matching circuits must transform the complex conjugate of the transistor large-signal input and output impedance values to the 50 Ω seen at the signal generator, and RF load. In so doing, one must keep in mind that the impedance values will vary with bias point and from device to device, and that the numbers provided by the device data sheet are only typical. We allowed for such variability with an impedance transformer consisting of a shunt capacitor placed at an adjustable position along the input and output 50-Ω microstrip lines. On the first design pass, we start with an equation for line impedance:

$$Z(L) = Z_0 (Z_{LOAD} + jZ_0 \tan\beta L)/(Z_0 + jZ_{LOAD} \tan\beta L)$$

where Z_0 is the characteristic line impedance, Z_{LOAD} = C in parallel with the RF input or output load (i.e., $R/(1+j\omega RC)$, β is the propagation constant, and L is the physical length between the device and the shunt capacitor. Z (L) is set to the complex conjugate of the impedance we wish to match to, i.e., $Z(L) = R_{in/out} + jX_{in/out}$. Using the above equation in this form, separated into real and imaginary parts, capacitance values and distances

close to those that are needed can be found. Since most high frequency capacitors come only in standard values, it is sometimes necessary to combine them in parallel to achieve the required values derived from the line equation. On closer examination, one must also account for the inductance presented by the capacitor leads. This series inductance, usually on the order of a few nH, is large enough to yield an improper match if ignored. Once all this has been taken into consideration, and theoretical values and distances have been found, the next step is to apply them to the test fixture. Allowing for variation in capacitance values due to tolerances, and variation in the lead inductance due to varying lead length is necessary, and the desired transformation must be confirmed by testing for the new impedance values once the components are in place. In this case, initial capacitance values and distances were tested and chosen based on a combination of theoretical results from the line equation, and Impedance values taken from a VNA. Once the capacitors are in place along the test fixture, and the desired transformation has been confirmed, the SSPA gate and drain are biased through external bias tees and the RF signal is applied to the gate. At this point, if the SSPA is seen to be amplifying, the matching circuit is fine-tuned by moving the capacitors along the microstrip line while looking for peaks in output power. As a result of this methodology, on the input circuit a capacitance of 15pf was placed approximately 15mm from the device, and on the output circuit two capacitances of values 7.5 and 8.2 pF were placed in parallel approximately 19.2 mm away from the device. The capacitors in place along the test fixture can be seen in Figure 9. These values and distances combined to yield a transformation from 50 Ω to 1.0 + 8.1j on the input, and 2.8 + 5.5j on the output. Once the device is confidently matched, the next step is to prepare it for spray cooling with water. This preparation

consists of removing the ceramic lid to the device package and coating the top surface of the Si die with Parylene-C – a conformal polymer having excellent dielectric strength and low relative permittivity. Such a coating is necessary to spray cool with water, which if allowed to strike the transistor surface directly, would likely short out the device. The Parylene thickness of 3.0-μm is chosen to be thin enough to not significantly impede the heat transfer, but thick enough to prevent shorting.

D. Design of Spray Nozzle

Our spraying approach was carefully chosen to minimize overall package volume and to take advantage of the high convective heat capacity and latent heat of vaporization of water – still one of the best, if not the best, choices for spray cooling in the range of ~100 to 150°C. It has been reported that at the micro-electronic chip level, the two best approaches to heat removal are through jet spray cooling, and atomized spray cooling.[i] Of the cooling approaches reviewed, these two approaches offer the highest heat removal with atomized spray reported at a critical heat flux of 0.6 kW/cm^2, and Jet boiling on a micro-surface reported at 0.5 kW/cm^2.[ii] For this experiment, we chose an orifice style jet-impinging scheme, without atomization, based on its ability to remove a significant amount of heat while minimizing the necessary pumping power. The orifice plate, specifically without additional atomization, has been observed to be more efficient, in terms of energy going into and out of the cooling setup, than various other nozzles, in the application of chip level cooling.[iii] This is in part because in order to atomize the stream, extra energy must be added into the system that will break the stream into microdroplets. In order to allow the usage of water and to control the position of spray streams from a

nozzle at the micron scale of RF transistors, we opted to fabricate the nozzle by bulk micro-machining from a 200-micron-thick silicon wafer. This entailed two key steps in fabrication: (1) patterning holes in photoresist thick enough (~5 micron) to act as a mask for reactive-ion etching (RIE), and (2) a long period (~3 hours) of RIE to chemically etch through the entire Si substrate. The chemistry of the RIE is known to sustain a highly anisotropic etching action so that the resulting holes have nearly perfect vertical sidewalls.

To help minimize the spraying rate, we tailored the design of the nozzle to the heat source distribution of the transistor under test, an LX-401 LD-MOSFET manufactured by Polyfet RF Devices.[iv] Fig. 11 shows the two-dim array holes in the micro-nozzle: 28 holes along the horizontal axis, and 18 holes along the vertical axis. Each hole has a 35-micron diameter and the center-to-center spacing is 180 micron along the x-axis and 90 micron along the y-axis. This exactly matches the layout of active cells in the LX-401. In fact, most RF transistors are designed in such a cellular way to optimize power at high frequencies, so our approach is rather generic in applicability. The actual nozzle can be seen in Figure 12.

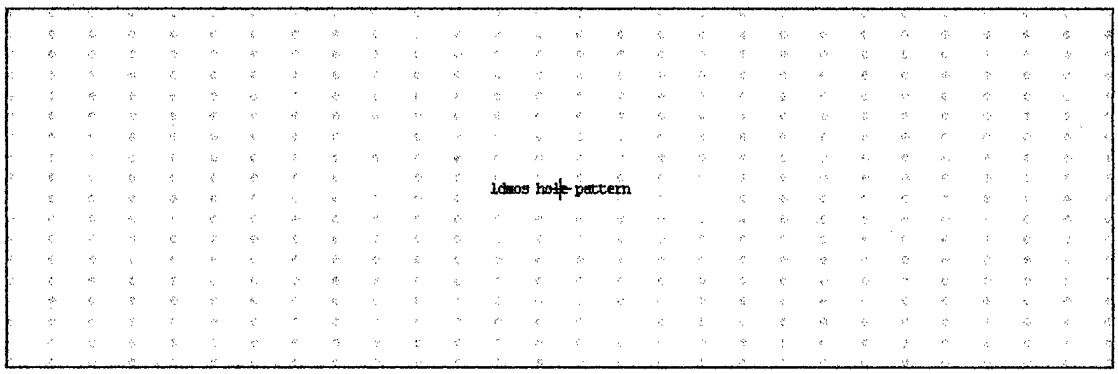

Fig. 11

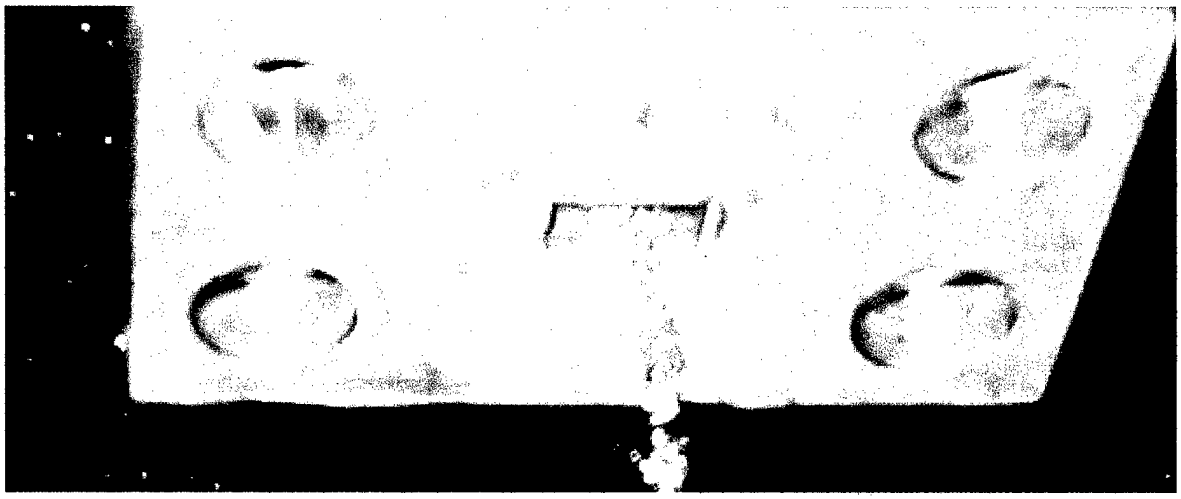

Fig. 12.

Fabricating a micro-nozzle from Si should also provide the following benefits. First, the reactive-ion etching of the nozzle orifices produces very smooth sidewalls compared to any known mechanical machining, so that the orifices have less of a tendency to trap contaminants and become clogged. Second, being made of Si rather than metal, the micro-nozzle is expected to be more chemically robust with respect to acids and other harsh chemicals that so often result from the leaching action of water.

Finally, fabrication from Si should be more affordable in mass production than competitive machine-shop or laser-drilling techniques, in spite of the long time required for the RIE step. This is because thousands of such nozzles can be fabricated simultaneously in each Si wafer (e.g., 8-inch diameter) in the same type of batch processing utilized in all garden-variety CMOS, MEMS, and other Si devices.

E. Experimental results

Shown in Figs. 13(a) and (b) are the output power (P_{out}), and power-added-efficiency (PAE) of the LD-MOSFET amplifier in class A operation (V_{gate} =3.6V) with and without spray cooling. As seen in Fig. 13(a), without spray cooling the device reaches a maximum output of 74 W at an input of 23 W. Between 15 W and 23 W input, the device appears to be nearly saturated and the Pout increases by only 4%. Above 23 W input, the device begins to break down, and the Pout drops off precipitously.

At the same gate and drain voltage, the spray cooling was then activated at a rate of 140 mL/minute and the device performance re-measured. The improvement can again be seen in Figs. 13(a) and (b). Between 5 and 23 W input, the output with spray cooling increased 5 to 10%, consistent with the already-efficient operation of the device over this range without spray cooling. However, above 23-W input where the unsprayed amplifier begins to break down, the spray-cooled device continues to operate without problems, providing steadily increasing output up to a measured maximum of 84 W at 34-W input. This is 27% higher than the unsprayed Pout at the same input 34 W input.

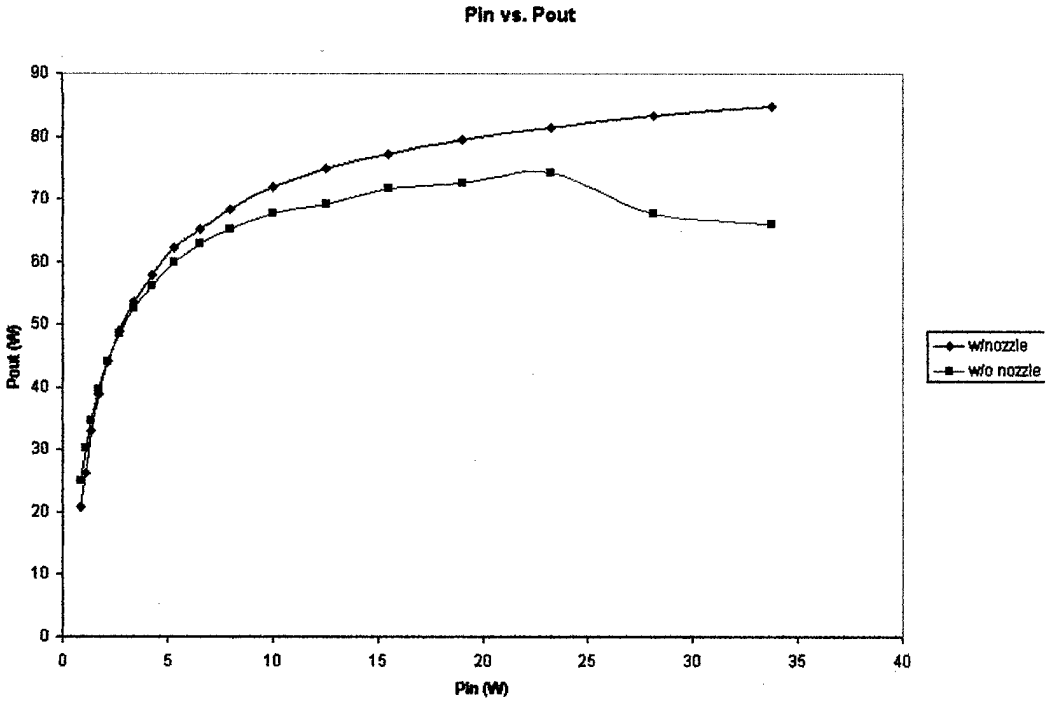

Fig. 13(a)

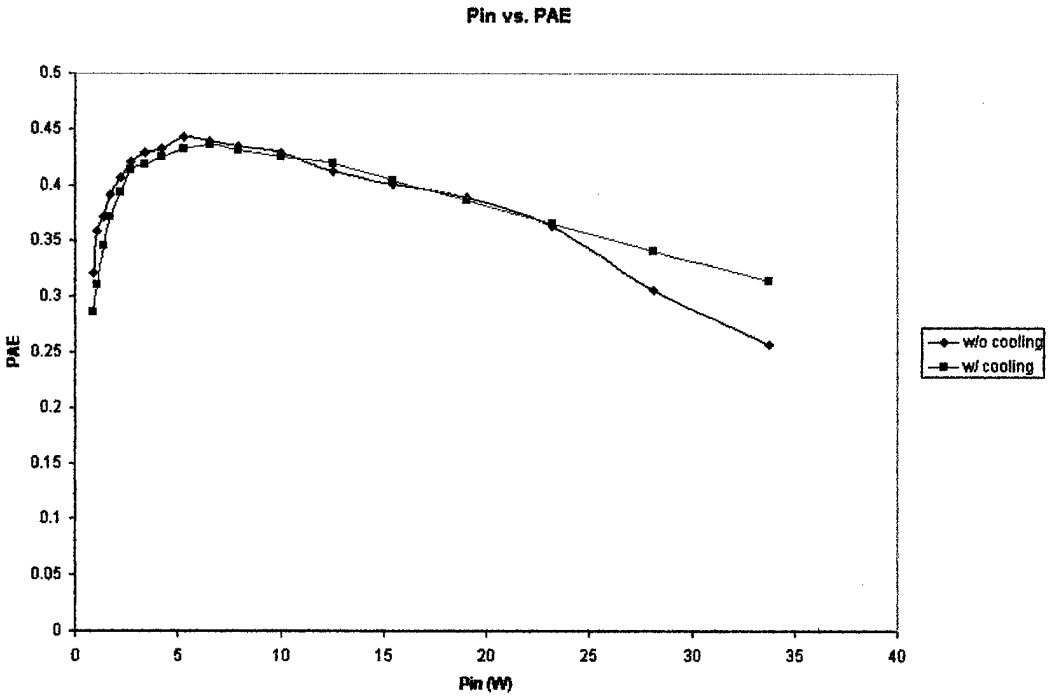

Fig. 13(b)

In terms of PAE, both the sprayed and unsprayed devices yield very similar results below 23 W input, but the spray cooling improves the efficiency significantly beyond this point. Graphs of PAE vs Pin can be seen for both cases in Fig. 13(b). Since the fundamental limit for PAE in class A is 50%, and the unsprayed device is already operating at about 40 to 45% from 1 to 15 W input, little improvement is expected over this range. The PAE peaks at 44% and 43% for the unsprayed and sprayed devices, respectively, both occurring at 5.3 W input. However, at 34 W input the unsprayed device PAE drops to 26% whereas the spray-cooled PAE is maintained at approximately 34 %.

The same experiment was also performed in class AB (V_{gate} = 2.6 V), yielding the plots of Pout and PAE vs Pin in Figs. 14(a) and (b), respectively. In this case, without cooling and at an input of 15 W, the device Pout peaked at 72 W. After this point, the Pout began to drop rapidly, and just beyond 18.5 W input and 70W out, the device self-destructed. With the spray cooling applied, the device ran without breaking down at much higher input powers, but didn't exhibit the marked increase in Pout as seen in class A. On the low end, from 1 to 5W in, and 25 to 62 W out, the increase in Pout ranges from 11% at 1.6W in to 2.3% at 5W in. From 5 to 15W in, and 60 to 70W out, the percent increase in Pout stays fairly flat at about 2%. After 15W in, the un-cooled device begins to break down, and by 18W in, the un-cooled device is putting out about 70 W, while the cooled device is putting out about 75W, a gain in power of 8%. By this point, the cooled device is mostly saturated, but is still able to operate up to 35W in, 79W out. Unlike the previous case of class A, when looking at the PAE of these two configurations

in the normal range of operation, some improvement can be seen. A graph of PAE vs Pin is shown in Fig. 14(b). The efficiency in both cases peaks around 4W in. At this input power, the un-cooled device runs at about 48%, while the cooled device runs at 52%. After this point, the PAE steadily decreases to the point where the un-cooled device breaks down, at which point it is running at a PAE of 40%. From 4W in, to 18W in, the cooled device steadily runs with a PAE about 3% higher than the un-cooled device.

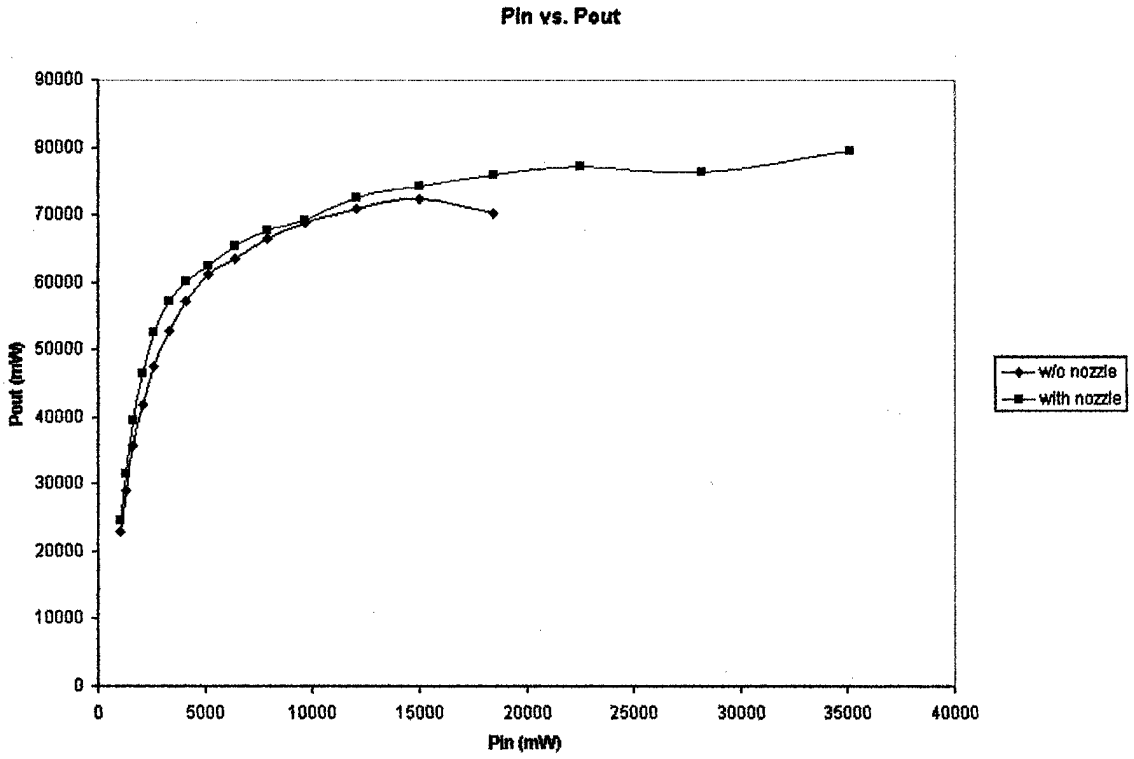

Fig. 14(a).

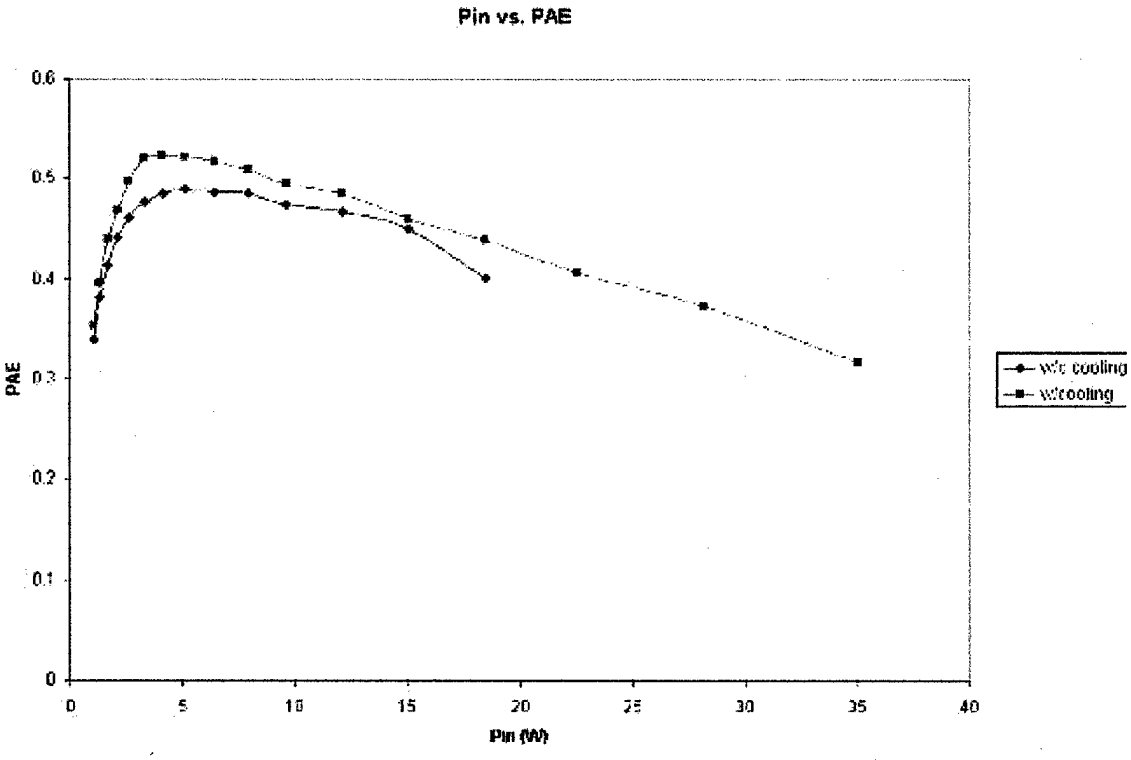

Fig. 14(b)

F. Summary and Conclusion

Upon examining the experimental results, it is evident that the improvement with spray cooling depends on how hard the device is being driven, and in which class of operation it is running. Since the class A device is always biased on, there is much more heat generated than in class AB at each value of Pout, and the device rapidly becomes more thermally limited. In this situation, spray cooling results in up to 27% improvement in Pout and an 8% improvement in PAE near breakdown. The PAE's in the range of common use are nearly identical. In class AB however, the device is biased off so that the area heat density is much lower, and the RF performance is less limited by thermal effects. Our spray cooling results in class AB therefore shows only an 8% improvement in Pout and a 3% improvement in PAE. However, class AB operation without spray cooling exhibits precipitous self-destruction that is mitigated significantly by the spray cooling. This suggests that the self-destruction is caused by a combination of electrical and thermal effects, and the spray cooling may help to improve the reliability of SSPAs in class AB operation. Further research on this issue is in progress.

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[i] Chunlin Xia, Spray/Jet Cooling for Heat Flux High to 1kW/cm^2, proc. 18th IEEE SEMI-THERM Symposium, pp. 159-163, 2002

[ii] Chunlin Xia, Spray/Jet Cooling for Heat Flux High to 1kW/cm^2, proc. 18th IEEE SEMI-THERM Symposium, pp. 159-163, 2002

[iii] Shanjuan Jiang, Heat Removal Using Microjet Arrays and Microdroplets in Open and Closed Systems for Electronic Cooling, Ph.D dissertation, UCLA, 2002

[iv] Polyfet RF Devices, www.polyfet.com

FINAL REPORT

for

HERETIC – HEAT REMOVAL BY THERMO-INTEGRATED CIRCUITS

Covering the Period
October 21, 1999through September 30, 2002

Presented to the
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Executive Summary

The combination of high power dissipation (e.g., >500 W) and high power densities required of power conversion devices, such as those utilized within variable-speed motor drives, necessitates thermal management systems with ever-increasing capabilities. Although device power densities on the order of 100 W/cm^2 are relatively common in applications today, technology roadmaps project power densities in excess of 1 kW/cm^2 within a few years. Unfortunately, conventional thermal management schemes result in excessive junction temperatures under these extreme conditions. Consequently, the role of passive and active cooling of high heat flux silicon-based power devices within variable-speed AC motor drives was explored with water as the phase-changing medium within the present program. Specifically, both heatpipe-based systems and direct spraying methodologies were studied. Heatpipe-based systems were found to offer only comparable performance to solid-state conduction based thermal management systems; however, direct spraying of the active electronics was found to result in a significant reduction of the junction temperature of the electronics at comparable power dissipation levels. Furthermore, this latter result was obtained from direct measurements while in-situ within a three-phase AC induction motor system operating under an 18 hp applied load.

In the first phase of the program, three categories of power modules were designed, fabricated and evaluated for the purpose of characterizing the thermal transport characteristics of planar heatpipes fabricated by Thermacore. The investigations included experimental measurements coupled with analytical and numerical determinations of thermal response. The first category of power module was fabricated according to current assembly practices, whereas the second category included a large piece of solid copper in the same location and with the same dimensions as the heatpipes that were included in the third category. In turn, the dual purposes of the copper block were to explore the phenomenon of heat spreading as a means of reducing the thermal resistance of electronic packages and secondly, to provide a baseline of data against which to quantitatively evaluate the effective thermal conductivity of the heatpipe.

The specimens containing the copper block were found to consistently exhibit a lower thermal resistance than those fabricated according to standard approaches. Both detailed, three-dimensional numerical analysis and simple analytical analysis of the experimental specimen and results confirmed that this resulted from the decrease in thermal resistance through heat spreading associated with the copper block. Furthermore, the specimen containing the heatpipe exhibited a relatively high thermal resistance as compared to the other two types of modules, but one that dramatically decreased with increasing power dissipation and hence temperature. This was correspondingly interpreted to indicate a non-optimized internal structure within the heatpipe, but one that did exhibit the anticipated highly non-linear trend in thermal resistance resulting from the onset of boiling/recondensation and capillary pumping of the working fluid within the heatpipe.

In the second phase of the program, direct spray-cooling of the electronics was investigated. Issues that were addressed include the packaging of a nozzle array design in a high-power module (> 650 W dissipation) that operates with high standoff voltages (V_{rms} ~ 325 VAC). Electrical isolation of the devices was achieved by a Parylene coating. An effective thermal resistance of ~ 0.007 C/W was achieved through direct water spray-cooling of the electronic devices. Finally, the calculated and measured spray-cooling thermal resistance is compared to those obtained in the first phase.

Section 1. Heat-Spreading Approaches for IGBT-Based Power Modules

1.1 Introduction

Insulated Gate Bipolar Transistor (IGBT) - diode power modules are used for high power inverter and converter applications such as motor drives and power supplies. These applications typically operate at high power levels (>1000W) and dissipate power in the form of heat owing to small device inefficiencies, typically on the order of a few percent. To minimize the consequent rise in temperature of these devices, the thermal resistance of the structure should be small. In the present investigation, a range of heat-spreading structures, including heatpipes, are explored as a means of reducing the thermal resistance of high-power packages for motor drive inverter modules. In the following sections, the design and fabrication of the specimens are described, followed by a description of the experimental approach and a presentation of the results. Then, the results of a simple analytical treatment are presented that rationalizes these results, followed by a section describing a three-dimensional analysis of the structure.

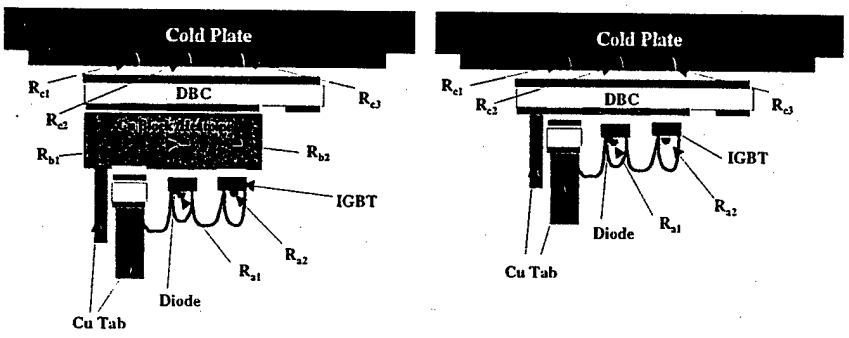
1.2 Specimen Geometry and Experimental Configuration

Silicon insulated-gate, bipolar transistor (IGBT) / diode modules were developed and evaluated experimentally, numerically and analytically. A schematic of the geometry of the specimens and experimental configuration is shown in Fig. 1. Electrically, the specimens correspond to a simple forward biased IGBT with a diode in parallel. Physically, the modules are based upon direct-bond copper (DBC) substrates. Three types of modules were prepared and are distinguished by the structure of the module immediately below the device:

(i) Devices that are soldered directly to the DBC substrate, designated "DBC modules" (Fig. 1 (b));

(ii) Devices that are soldered directly to relatively thick (6 mm) copper blocks that are inserted between the device and the DBC substrate, designated "Copper-block modules" (Fig. 1 (a));

(iii) Devices are soldered to a relatively thick (6mm) planar thermosiphon heatpipe fabricated by Thermacore, designated "Heatpipe modules" (Fig. 1 (a)).



(a) (b)

Fig. 1. Schematic of the test specimens and experimental geometry. (a) Cu-Block or Heatpipe IGBT-Diode Module; (b) DBC IGBT-Diode Module. The names of the constituents are indicated along with the positions of the RTD temperature sensors as described in the text.

The copper blocks in (ii) are of identical dimensions and in the same physical location as the heatpipes in (iii) and thus represent a comparative baseline. Photographs of the DBC and Cu-block specimen types are shown in Fig. 2.

The goal was to measure the spatial distributions of temperature throughout the modules and baseplate at positions determined in agreement with colleagues at UCLA. Temperatures were measured utilizing RTD sensors from Omega that were cemented into position as a function of power dissipated within the devices. The attachment of RTD's to the different areas in the modules was done with Omegabond 400 cement. The locations where RTD's were attached are shown in Fig. 1(a) for the Cu-Block and heatpipe modules and Fig. 1(b) for the DBC module. A total of four RTD measurements were taken while measuring on the DBC module and six on the Cu-Block and heatpipe module. The three RTD's attached to the coldplate are designated as R_{c1}, R_{c2}, and R_{c3}. The two RTD's on the copper block/heatpipe are designated as R_{b1}, and R_{b2}. The RTD attached to the diode is designated as R_{a1} and the one attached to the IGBT as R_{a2}. The RTD aligned with the device measures case temperature T_c and the one on the device measures the junction temperature T_j. During the experiments, the test specimens were clamped to a water-cooled copper baseplate using miniature C-clamps, and a thin layer of conducting grease was introduced to enhance thermal contact between the bottom of the test specimen and the chilled baseplate. The temperature of the water within the baseplate was regulated to 16°C with a high-power Neslab refrigerated recirculator.

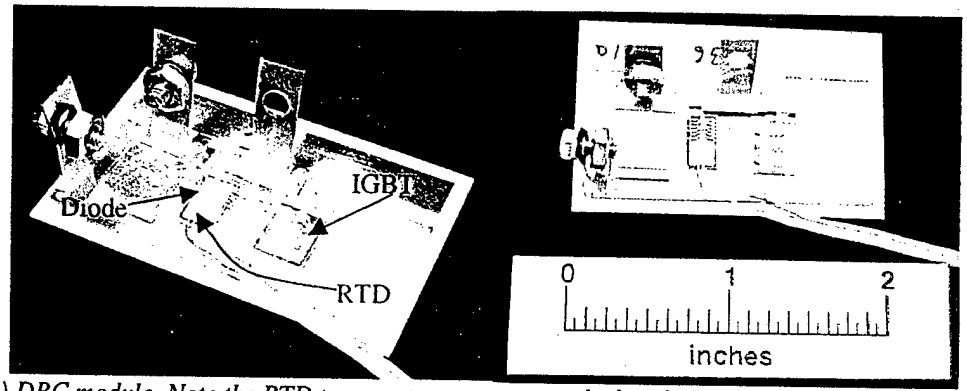


Fig.2 (a) DBC module. Note the RTD temperature sensor attached to the top surface of the diode.

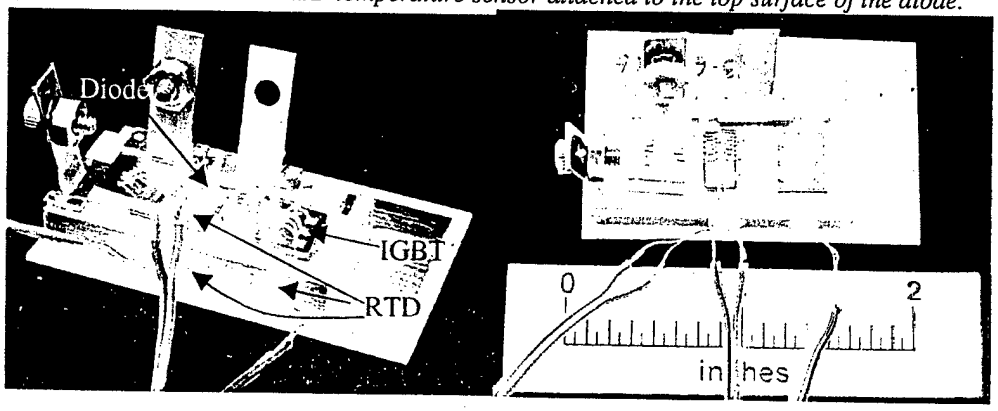


Fig.2 (b) Cu-block module. Note the RTD temperature sensors attached to the top surface of the diode, as well as various locations around the perimeter of the copper block.

All measurements of temperature, voltage and current were taken with an automated custom high-power test facility utilizing a National Instruments LabView based virtual instrument, where the experiments were performed in a current source mode with the diode current I_d sequentially stepped through the specified range. Here, experiments were performed over a current range of 0 – 50 A, in steps of 5A. The diode voltage drop V_d across the device was measured using a high precision voltmeter and Kelvin probes. The operator specified the interval of time at each current level.

1.3 Specimen Preparation

Packaging of the modules comprised design and fabrication of the constituents, acquisition of the devices, and then soldering and wirebonding assembly of the modules. The large dimensions of the heatpipes and large mismatches in thermal expansion coefficients posed unique challenges in developing a systematic packaging procedure that could be reliably implemented across the three categories of test specimens. Specifically, the soldering of the test modules was performed with several different solders materials and soldering conditions (See Appendix 1.1). Wirebonding was performed with 10-mil aluminum wire and an ultrasonic wedge bonding procedure. The complete summary of modules fabricated to date is provided in the Appendix.

In order to confirm the quality of the solder joints at the various interfaces within the power modules, a series of ultrasonic scans were performed at the RSC utilizing our high-resolution custom immersion ultrasonic system. For example, representative ultrasonic scans five layers (designated 1A, 1B, 1C, 1D, and 1E) were obtained for the Cu-Block module system, which was soldered with 96.5%Sn-3.5%Ag solder (Fig. 3 and Fig. 4). As seen in Fig. 4 the green areas show good solder bonds and the orange dots show voids.

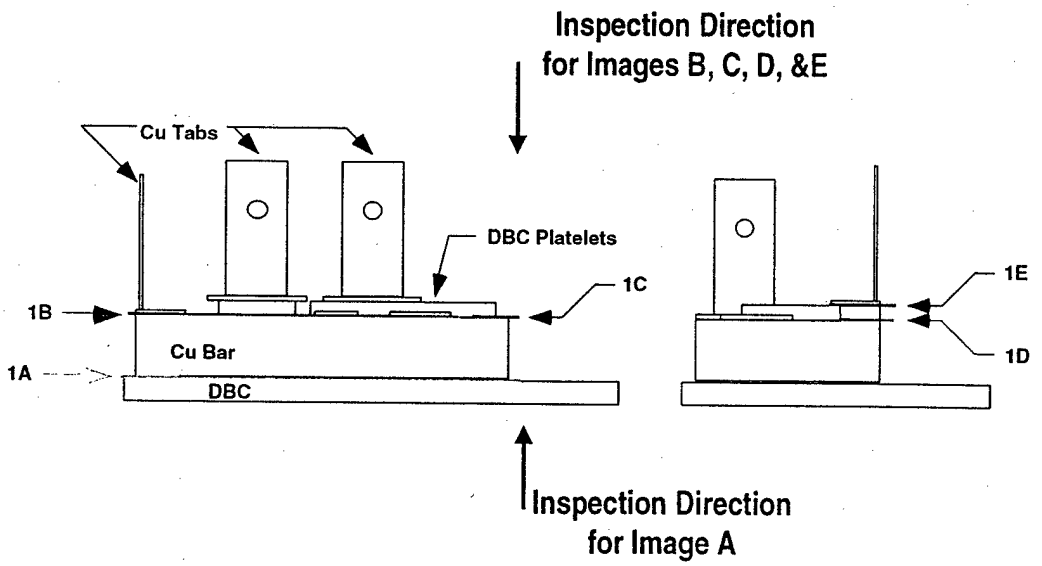


Fig. 3 Layers of the Cu-Block module analyzed by ultrasonic acoustic microscopy.

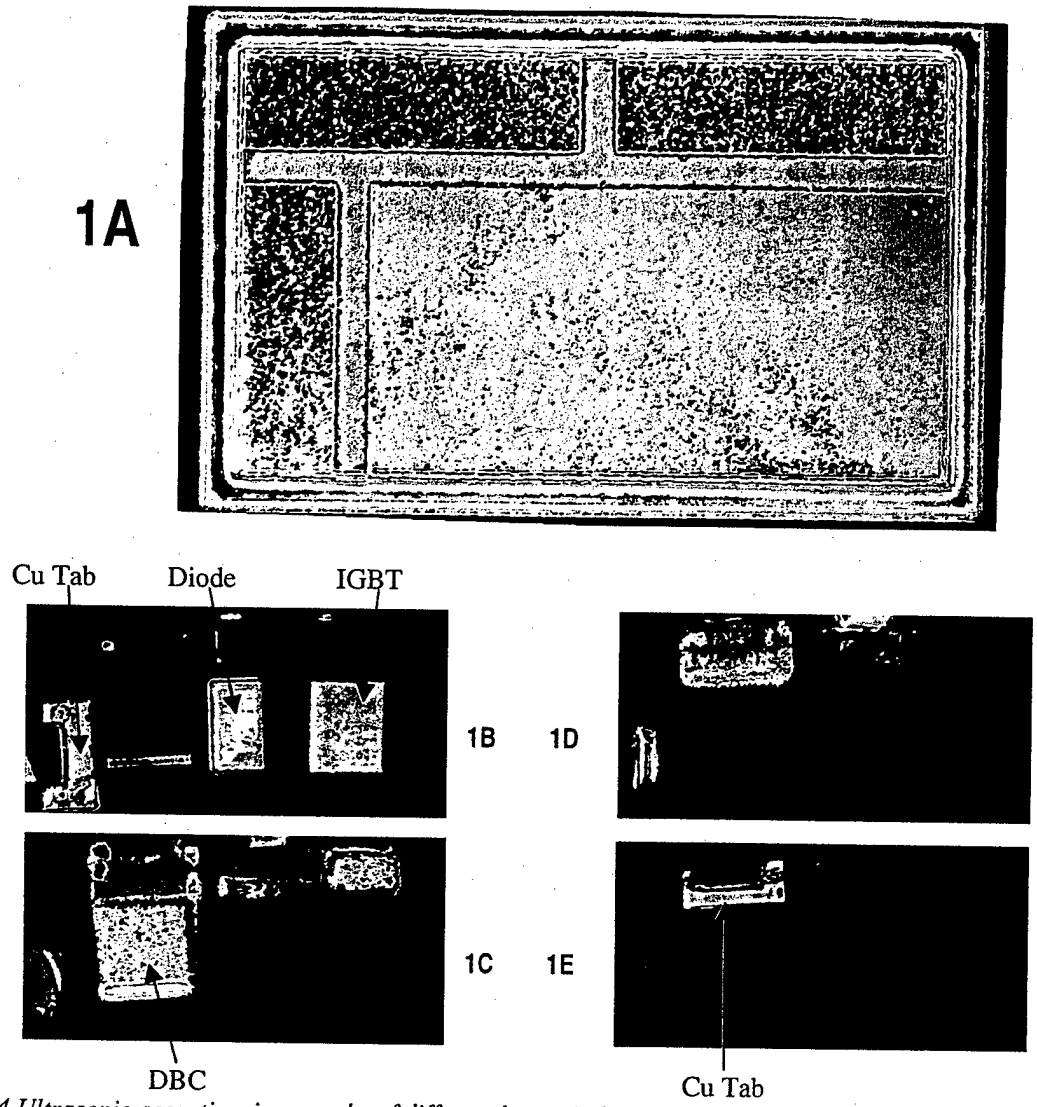


Fig. 4 Ultrasonic acoustic micrographs of different layers indicated in Fig. 3.

All the layers in Fig. 4 show good solder bonds except the interfaces under the device, which exhibited several voids. Therefore, the alternative system, 63%Sn-37%Pb, was investigated for various thicknesses of solder preforms (Fig. 5) for soldering the devices to the substrates. Although the 1 mil thick solder showed minor voids, the 2 mil and the 4 mil solder were essentially void free, although in the case of the 4 mil solder, excess solder was observed around the perimeter of the device that jeopardized its subsequent high-voltage standoff capability. Based on these observations, soldering of the devices was done with 2 mil 63%Sn-37%Pb, whereas soldering of the rest of the assembly was performed with 96.5%Sn-3.5%Ag solder. I.e., all the modules were soldered in two steps: In step 1, everything except the devices was soldered with 2 mil 96.5%Sn-3.5%Ag, and in step 2 the devices were soldered with 2 mil 63%Sn-37%Pb. The wirebonding was then performed with 10 mil 99.99% Al wire; the RTD's were cemented with Omegabond 400 cement and cured for 4 hours at 80°C.

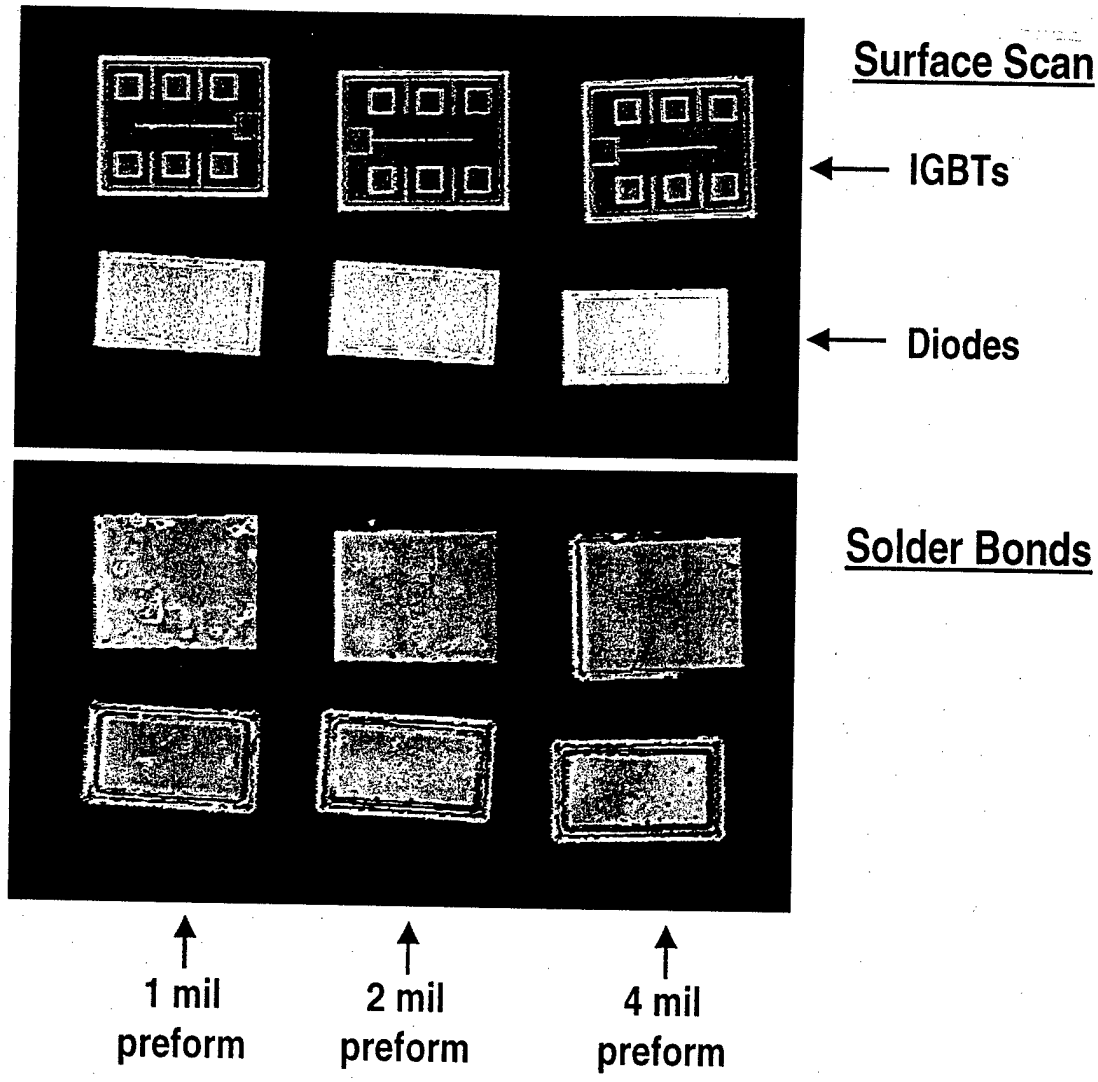


Fig. 5 Ultrasonic acoustic micrographs of specimens prepared with 1 mil, 2 mil, and 4 mil thickness of solder. Based on these results, a 2-mil preform was selected for fabrication of the modules utilized within these experiments.

1.4 Experimental Results:

Temperature, voltage, and current measurements as a function of time were measured with the seven DBC, Cu-Block and Heatpipe modules described above. Each module was tested three times, including complete disassembly and reassembly of the clamped configuration. I.e., for the three DBC and three Cu-block modules, there were a total of nine data sets (18 total) whereas for the single heatpipe module there was a total of three data sets.

Representative data for voltage, current and junction/baseplate temperatures from one of the DBC module experiments with diodes are shown in Fig. 6, and from one of the Cu-block module experiments in Fig. 7. Initial measurements were obtained at 60-sec intervals for 60 minutes for each current level. The voltage and temperature reached

steady-state levels after approximately 3 minutes at low current and 5 minutes at higher levels of current. Based on these observations, all subsequent readings were recorded every 30 seconds for 15 minutes intervals at each current level. All temperature measurements were performed with the diodes; temperature measurements utilizing the IGBTs were problematic, as described in Appendix 2. (Also shown in Figures A.1 and A.2 in Appendix 2 are shorter time period segments of the experiments described in Figs. 6 and 7 with an expanded vertical axis, wherein the stability of the diode voltage and temperature readings are clearer than in Figs. 6 and 7.) Finally, typical temperatures at the diode and baseplate RTDs as a function of dissipated power during the experiments are illustrated in Fig. 8.

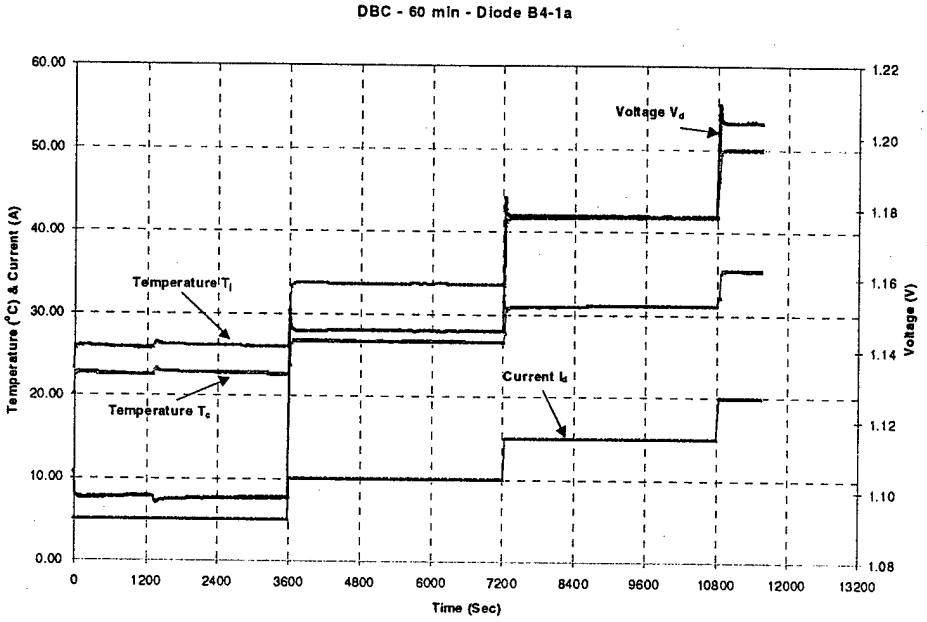


Fig. 6 Typical example of current, voltage and temperature measurements for diode on DBC.

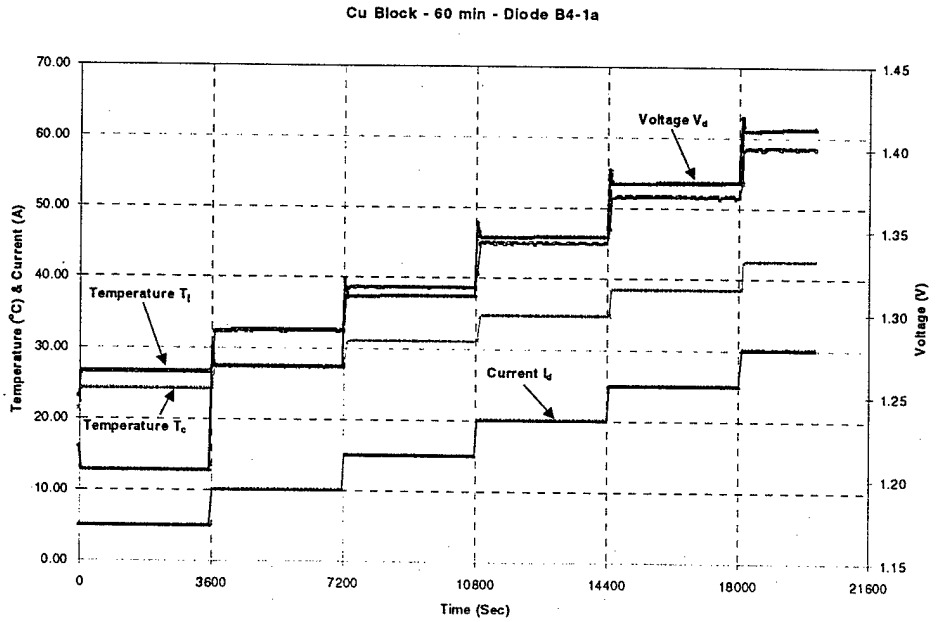


Fig. 7 Typical example of current, voltage, and temperature measurements for Diode on Cu-Block.

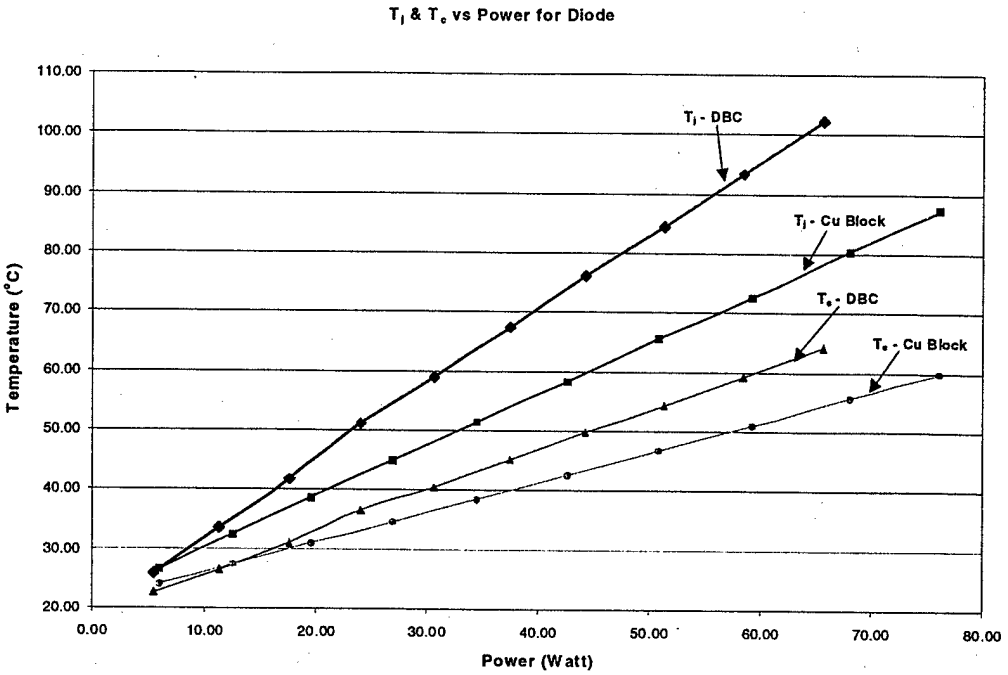


Fig. 8 Summary of selected temperature measurements vs. dissipated power.

These data were then analyzed for thermal resistance, R_{th}, in accordance with:

$$R_{th} = \frac{T_j - T_c}{P_{diss}}$$

where P_{diss} = Dissipated Power

$$= V_f * I_f$$

Results for thermal resistance as a function of dissipated power are shown for the complete sets of data in Fig. 9 for the DBC modules, Fig. 10 for the Cu-block modules and Fig. 11 for the Heatpipe module. A summary of these data is provided in Fig. 12, along with analytical predictions for the thermal resistance from the following section.

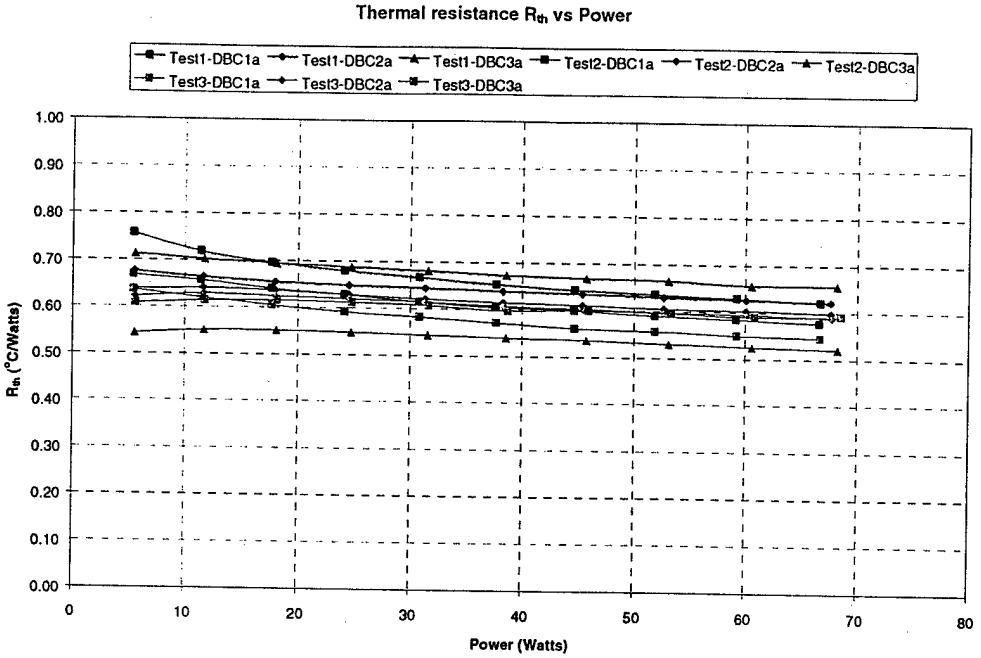


Fig. 9 Thermal resistance for DBC modules as a function of power dissipated in the diode.

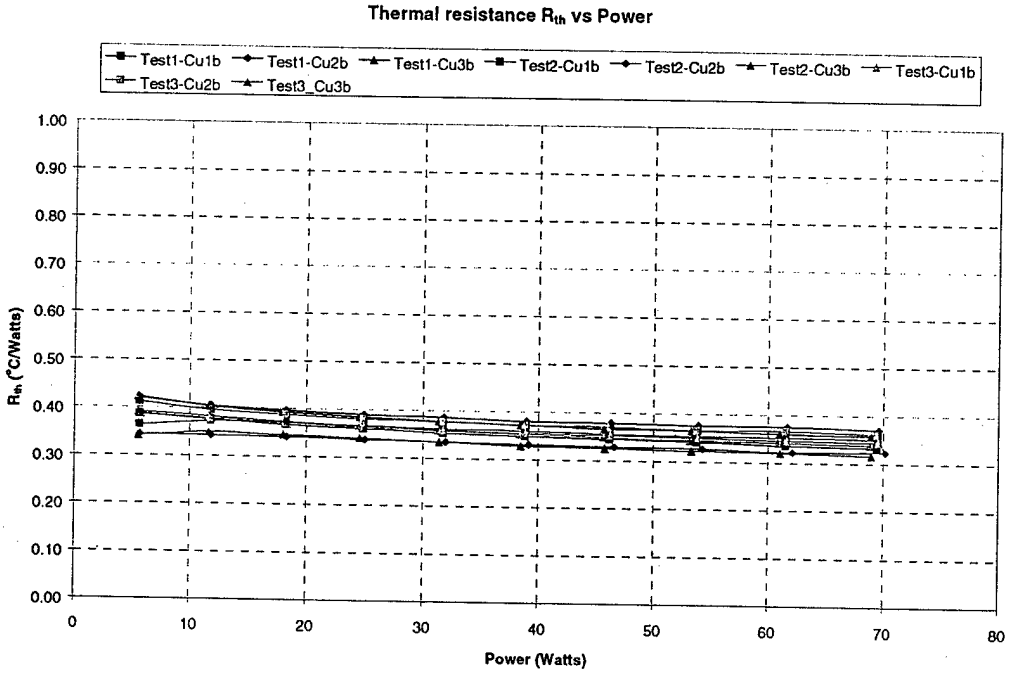


Fig. 10 Thermal resistance for Cu-block modules as a function of power dissipated in the diode.

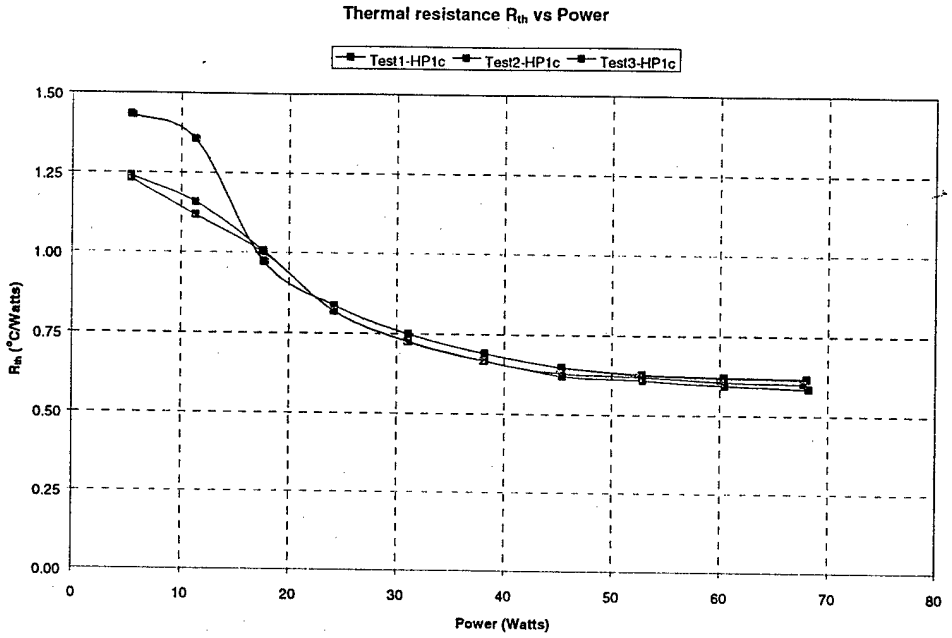


Fig. 11 Thermal resistance for the heatsink module as a function of power dissipated in the diode.

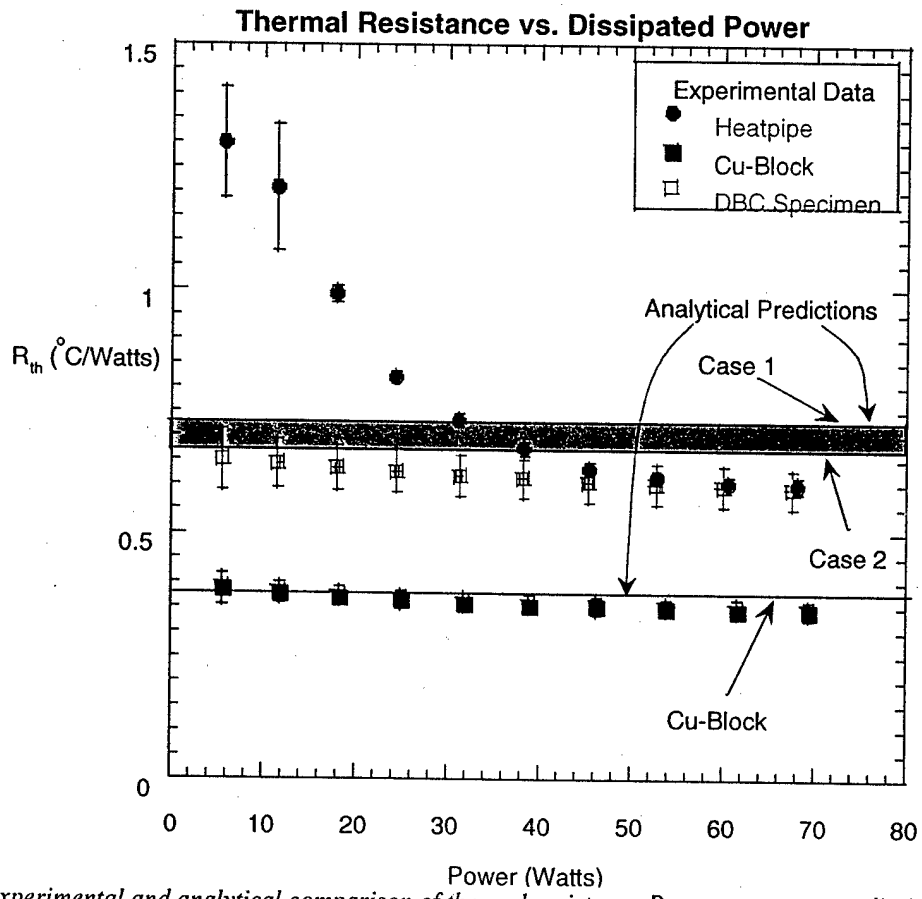


Fig. 12 Experimental and analytical comparison of thermal resistance R_{th} measurement vs. dissipated power.

Based on these results (Fig. 12), the following conclusions may be drawn:

1) The thermal resistance of the copper-block module is less than that of the DBC module.
2) The thermal resistance of both the copper-block and DBC modules is essentially invariant with dissipated power/temperature
3) The scatter in the experimental results is typically less than 5-10%.
4) The thermal resistance of the heatpipe module is greater than both the copper-block and DBC modules, except at higher levels of power dissipation.
5) The thermal resistance of the heatpipe changes by almost a factor of two over the range of dissipated power.

These conclusions are now explored within the context of the analyses in the next two sections.

1.5 Analysis - Analytical:

In this quasi-analytical analysis, the following assumptions were made.

- For the case of the DBC module, the heat transfer is essentially one dimensional with limited spreading (Fig. 13). Therefore, the determination of R_{th} for each layer is:

$$R_{th} = \frac{l}{kA}$$

where l = Length of heat transfer path, m

k = Thermal Conductivity, W/m K

and A = Area, m^2

- Also for the DBC module, since the diode dimensions are 4 mm x 7.7 mm, two limiting cases were analyzed. In the first, the model comprises a single square diode having the same side dimension (5.5 mm) as a square with the same area as the diode. In the other limit, the model assumes that two parallel squares operate, each with a side dimension of 4 mm.
- For the Cu-Block module, a significant degree of heat spreading takes place, owing to the comparable thickness of the copper as compared to the lateral dimensions of the diodes, coupled with the order-of-magnitude difference in thermal conductivity between the copper block heat spreader and the alumina baseplate. Therefore, the appropriate model for thermal resistance includes full heat spreading within the copper block [Tummala] and one-dimensional heat flow elsewhere (Fig. 14):

$$R_{th} = \frac{H}{ka\pi}$$

where H = Spreading Resistance Factor

k = Thermal Conductivity of copper, W/m K

and a = Radius of the copper block, m

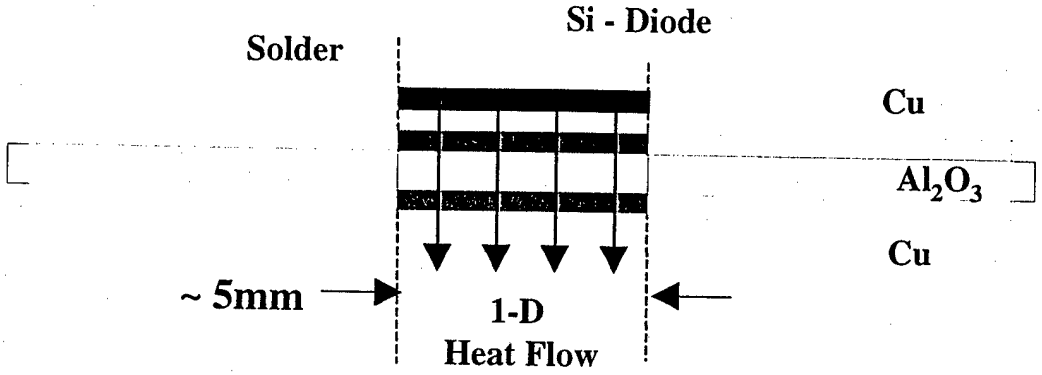


Fig. 13. Schematic of the one-dimensional analytical heat transfer model for the DBC module.

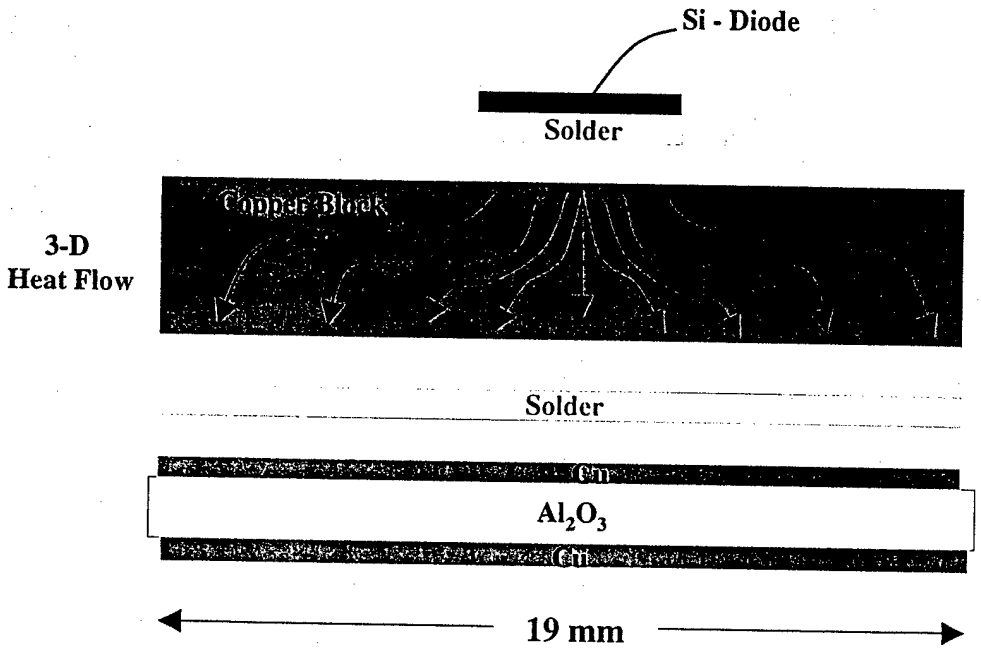


Fig. 14. Schematic illustrating the analytical heat transfer model for the copper-block module that includes two-dimensional heat-spreading within the copper block.

Based on these assumptions, the predicted thermal resistance for the DBC and copper-block modules is summarized in Table 1, and is indicated in Fig. 12 with comparison to the experimental data. Overall, the good agreement confirms the significance of the heat spreading phenomenon in reducing the thermal resistance of the copper-block module as compared to the DBC module.

Table 1

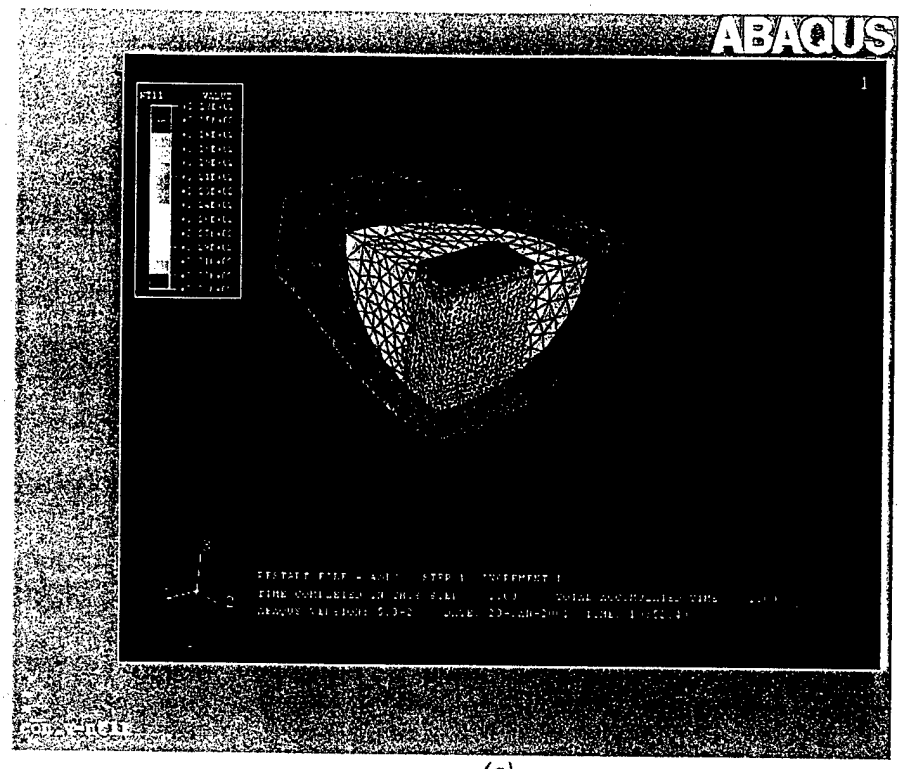
Case	Thermal Resistance R_{th}
DBC module – Case 1	0.721 °C/W
DBC module – Case 2	0.681 °C/W
Cu-Block module	0.375 °C/W

1.6 Analysis - Numerical

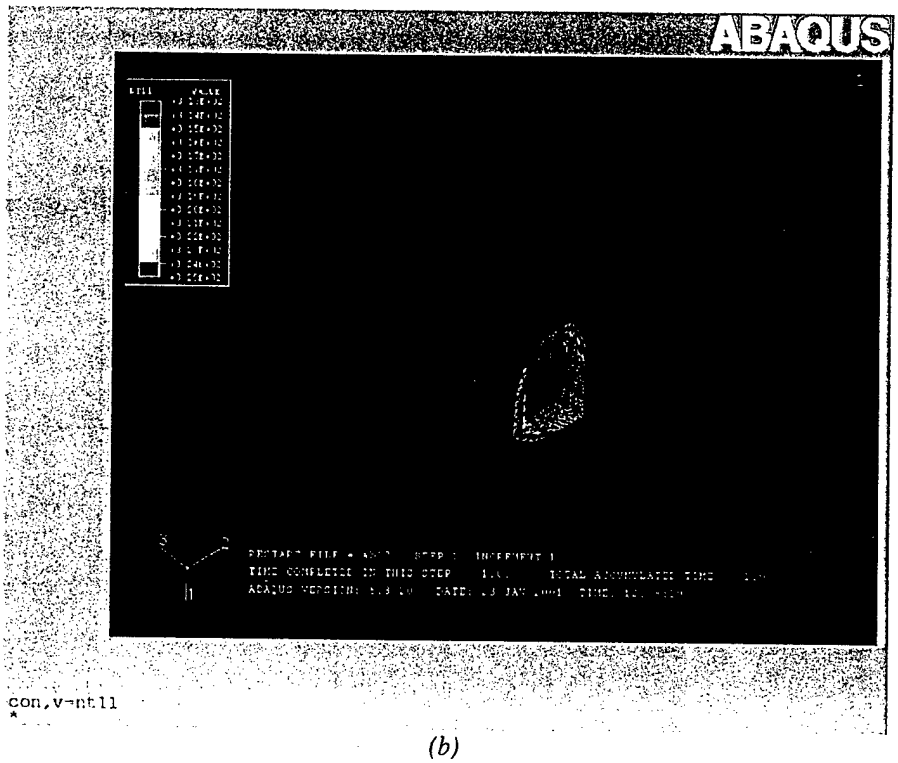
In order to further explore the origins of these differences in thermal resistance, a three-dimensional finite-element analysis was performed of both the copper block and DBC modules. Owing to symmetry considerations, one-quarter of the modules were modeled. The FEA program ABAQUS was utilized and the models comprised between 60,000 to 100,00 ten-noded tetrahedral elements with the diode subject to a volumetric power density corresponding to a net dissipation of 60W. The lower surface of the DBC substrate in both cases was fixed at 313K as a fixed temperature boundary condition. The remaining surfaces were insulated.

Contour plots of the results are illustrated in Fig. 15. The distinct difference in heat spreading between the two cases is clear. In the copper block case, Fig. 15 (a), a volume of the copper block with a radius several times the side dimension of the diode experiences an increased temperature associated with a corresponding decrease in heat flux from the diode source. In the DCB case, Fig. 15 (b), the region of the DBC that participates in heat spreading is confined to a volume with a radius smaller than the side dimension of the diode. Although the actual temperatures predicted by the copper block model are almost exactly identical to those measured experimentally and predicted analytically, there is a significant difference in the case of the DBC. This is believed to result from the departure from ideal fixed temperature boundary conditions in the experimental case, although this point requires further clarification. The key conclusion, however, which supports the analytical analysis, is that the degree of heat spreading between the two cases is sharply different, and that further activities are required to explore the response of the heatpipe with a more optimized working structure.

Finally, the observed thermal resistance behavior of the heatpipe module can be addressed. First, the substantial drop in thermal resistance of the heatpipe as a function of dissipated power is taken to correspond to the activation of the working fluid as the temperature increases over the range of dissipated power. Secondly, the high thermal resistance at low power is deemed to result from the low thermal resistance of a hollow copper shell, assuming that the working fluid is non-functional. Third, the asymptotic level of thermal resistance, ~0.6 °C/W, reached by the heatpipe at higher levels of power (> 60W, corresponding to a junction temperature of ~100° C), is still higher than that exhibited by the copper block module at the same power levels (~0.35 °C/W). This is concluded to result from a non-optimized wicking structure. Indeed, the "effective thermal conductivity" for the heatpipe, assuming that the heatpipe were a solid piece of material, can be calculated to be 190 W/mK, as compared to 400 W/mK for copper.



(a)



(b)

Fig. 15. Contour plots of distributions of temperature for a dissipated power of 60W for the copper-block module (a) and DBC module (b). One-quarter of the module is shown owing to symmetry considerations. Note the major difference in heat spreading between the two cases.

Appendix 1.1 Summary of Experimental Test Specimens

Case #	Sample Type	Devices	Solder	Soldering Conditions	Module Condition
B1-1a	DBC	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B1-1b	Cu Block	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B1-1c	Heatpipe	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B1-2a	DBC	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B1-2b	Cu Block	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B1-2c	Heatpipe	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B2-1c	Heatpipe	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	OK
B2-2c	Heatpipe	IGBT, Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	Reflow furnace, N2 & Flux -RMA, 2 steps	Leakage in the Heatpipe
B3-1a	DBC	Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	ATV furnace, N2, H2, 2 steps	cu tab did not solder in step 2
B3-2a	DBC	Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	ATV furnace, N2, H2, 2 steps	cu tab did not solder in step 2
B3-3a	DBC	Diode	80Au-20Sn -1mil, 63Sn-37Pb - 1 mil	ATV furnace, N2, H2, 2 steps	cu tab did not solder in step 2
B3-1b	Cu Block	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	IGBT got damaged - chipped
B4-1a	DBC	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	OK
B4-1b	Cu Block	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	OK
B4-2a	DBC	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	OK
B4-2b	Cu Block	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	Diode totally chipped off
B4-3a	DBC	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	OK
B4-3b	Cu Block	IGBT, Diode	80Au-20Sn - 1mil	ATV furnace, N2, H2, 1 step	Diode partially chipped off
1	Cu Block only	IGBT, Diode	63Sn-37Pb - 1 mil, no DBC	ATV furnace, N2, 1 step	OK
2	Cu Block only	IGBT, Diode	63Sn-37Pb - 1 mil, no DBC	ATV furnace, N2, 1 step	OK
3	Cu Block only	IGBT, Diode	63Sn-37Pb - 1 mil, no DBC	ATV furnace, N2, 1 step, Flux #5 RA	OK
6	DBC only	IGBT, Diode	63Sn-37Pb - 1 mil, no DBC	ATV furnace, N2, 1 step, Flux #5 RA	OK
4	Cu Block	IGBT, Diode	96.5Sn-3.5Ag - 4 mil	ATV furnace, N2, H2, 1 step	1 cu tab moved, but OK
7	Cu Block	None	96.5Sn-3.5Ag - 4 mil	ATV furnace, N2, H2, 1 step	Too much solder- DBC & Cu
8	Cu Block	None	96.5Sn-3.5Ag - 4 mil	ATV furnace, N2, H2, 1 step	Too much solder- DBC & Cu
9	Cu Block only	IGBT, Diode	63Sn-37Pb, 1,2 & 4 mil, no DBC	ATV furnace, N2, 1 step, Flux #5 RA	OK
B5-1a	DBC	IGBT, Diode	96.5Sn-3.5Ag - 4 mil, 63Sn-37Pb - 1 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-1b	Cu Block	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-2b	Cu Block	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-3b	Cu Block	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-1c	Heatpipe	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-1a	DBC	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-2a	DBC	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK
B6-3a	DBC	IGBT, Diode	96.5Sn-3.5Ag - 2 mil, 63Sn-37Pb - 2 mil	ATV furnace, N2, H2, Flux #5 RA in step 2	OK

Appendix 1.1 (cont.)

Case #	Test Condition	Test Results
B1-1a	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B1-1b	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B1-1c	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B1-2a	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B1-2b	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B1-2c	Elastic bands to cold plate	Diode calibration - ok, Diode test - ok, IGBT test - ok.
B2-1c	Elastic bands to cold plate	IGBT burned out
B2-2c	No test	
B3-1a	No test	
B3-2a	U-scan test, U-1a	Disbonds at corners of cu tab, & maybe under the diode
B3-3a	U-scan test, U-2a	Disbonds at most of cu tab1, & maybe under the diode
B3-1b	No test	
B4-1a	RTD attached, clamp to cold plate	RTD with Epoxy adhesive causes problem on device char.
B4-1b	RTD attached, clamp to cold plate	RTD with Epoxy adhesive causes problem on device char.
B4-2a		
B4-2b	U-scan test, U-5b	AuSn has some disbond areas, and it stresses the devices
B4-3a		
B4-3b		
1	U-scan test, U-1b	Disbonds under the diode
2	U-scan test, U-2b	Disbonds under the diode
3	U-scan test, U-3b	Flux helps in soldering devices
6	U-scan test, U-3a	Flux helps in soldering devices
4	U-scan test, U-4b	AgSn is the best for all
7	U-scan test, U-6b	Good Solder
8	U-scan test, U-7b	Good Solder
9	U-scan test, U-8b	2 mil & 4 mil solder are good. Some disbonds with 1 mil solder
B5-1a	RTD attached, clamp to cold plate	RTD with Epoxy adhesive causes problem on device char.
B6-1b	RTD attached, clamp to cold plate	All test for diode completed
B6-2b	RTD attached, clamp to cold plate	All test for diode completed
B6-3b	RTD attached, clamp to cold plate	All test for diode completed
B6-1c	RTD attached, clamp to cold plate	All test for diode completed
B6-1a	RTD attached, clamp to cold plate	All test for diode completed
B6-2a	RTD attached, clamp to cold plate	All test for diode completed
B6-3a	RTD attached, clamp to cold plate	All test for diode completed

Appendix 1.2 – IGBT / RTD Investigations

For the case of the IGBTs within the modules, it was found to be essentially impossible to obtain reliable measurements of junction temperatures utilizing RTD thermocouples. This was presumed to result from minor damage to the delicate IGBT device structure as a result of application of the epoxy and subsequent curing at elevated temperatures, which resulted in minor current leakage across the gate within the IGBT during operation. This phenomenon was very reproducible, with examples shown below in Figs. A.1 and A.2. I.e., for constant current I_c the voltage drop, V_d, or, V_{ce}, does not stabilize, even for times of up to 4 hours. For the IGBT, the gate-emitter voltage V_{ge}, was maintained at 15.004V ± 0.001V, and the forward voltage V_{ce} was measured for a given collector current I_c. In order to investigate this phenomenon in greater detail, four specimens were prepared and tested, two with IGBTs on copper blocks and two with IGBTs on DBC substrates. Within each set of two, an RTD was mounted on one of the specimens, but not on the other. The change in voltage drop, ΔV_d, or, ΔV_{ce}, was then monitored during power dissipation, and the results are shown in Fig. A.3. The voltage fluctuates less then 0.5mV for modules without RTDs attached on the IGBT, independently of the presence of Cu-Block, whereas ΔV_{ce} is seen to be increasing constantly and significantly with time for the modules with RTD attached to the IGBT using epoxy adhesive. These results indicate the deleterious effects of epoxied RTDs to IGBTs. Based on these results no further measurements of IGBT junction temperature T_j were performed utilizing RTD's.

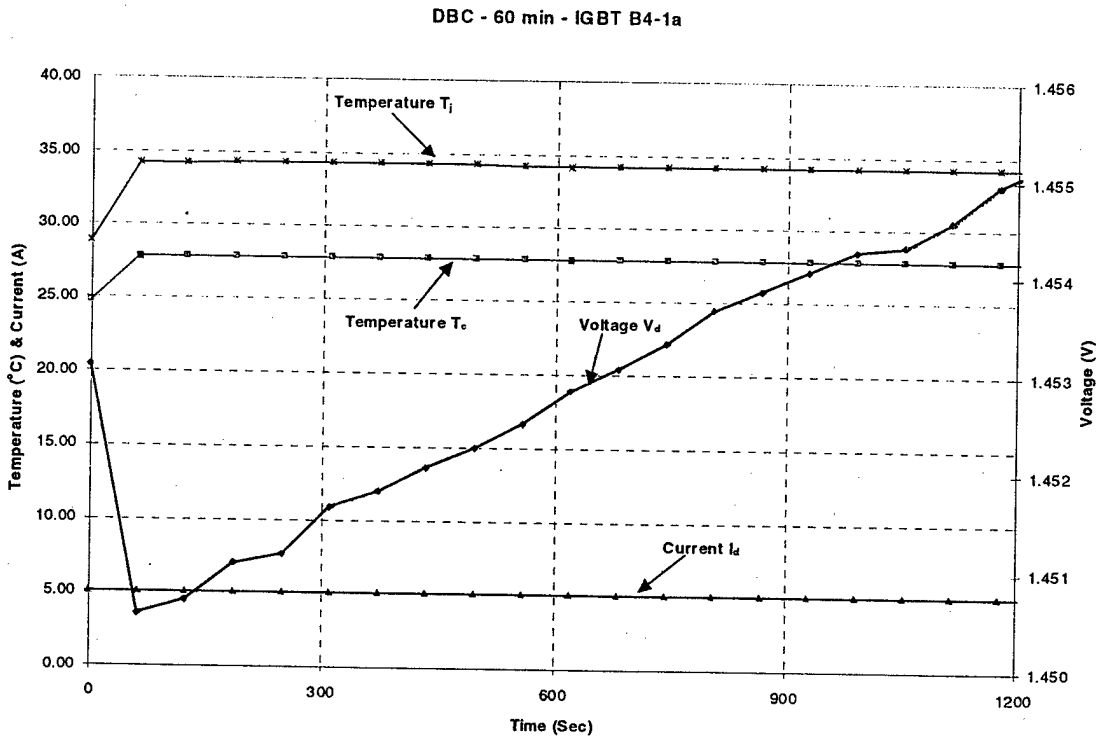


Fig. A.1 Current, voltage and temperature measurements for IGBTs on DBC, including an epoxied RTD.

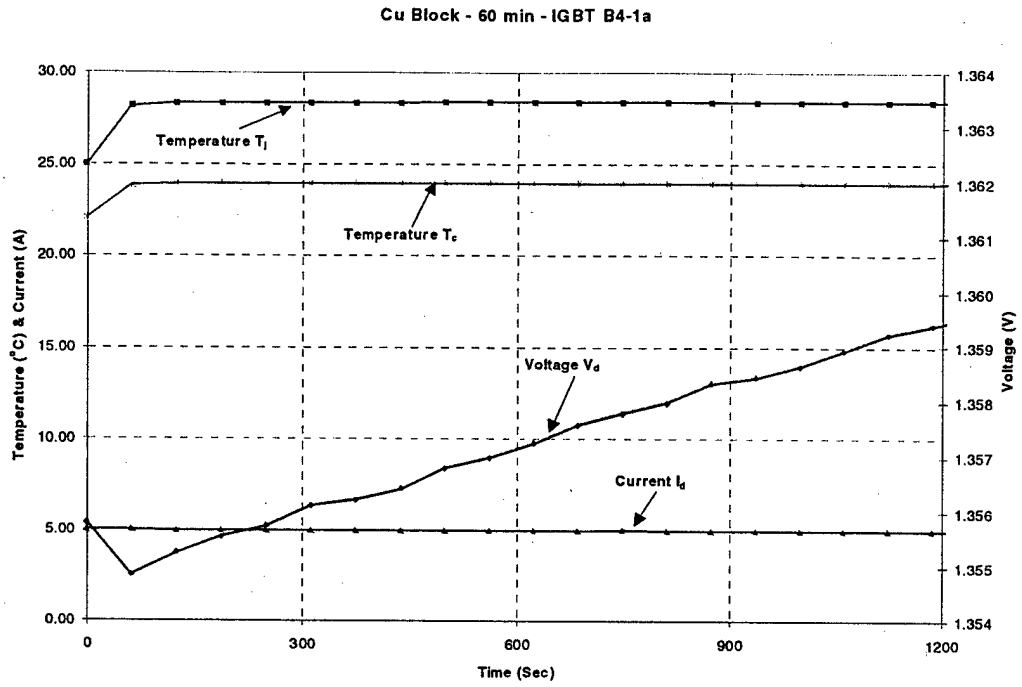


Fig. A.2 Current, voltage, and temperature measurements for IGBT on Cu-block, including an epoxied RTD.

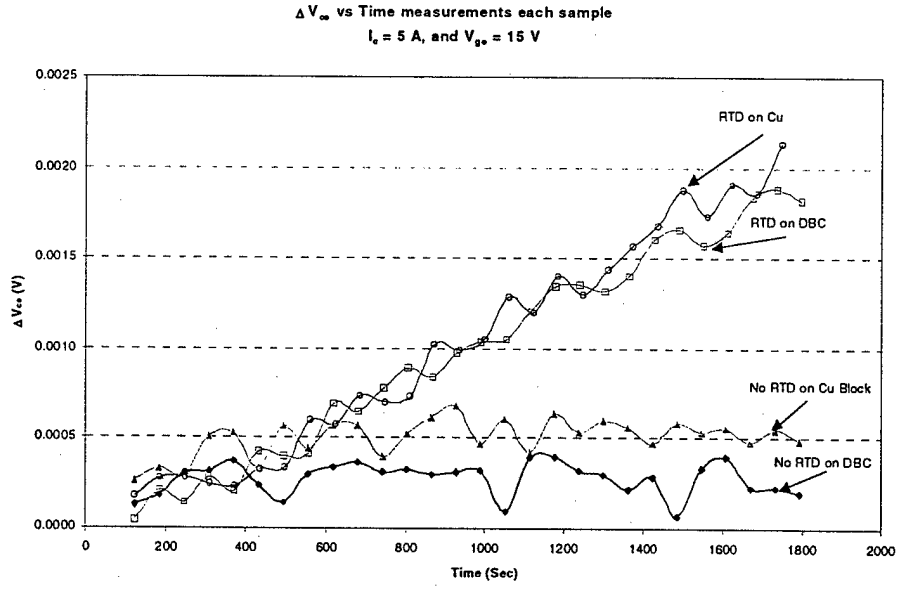


Fig. A.3 Plot of the change in V_{ce} as a function of time for specimens with and without RTD's on both copper block and DBS substrates. Note the relative independence of ΔV_{ce} with time for the IGBTs without the RTDs, irrespective of DBC or copper block substrate conditions, whereas the ΔV_{ce} consistently rises with time for the IGBTs with RTDs on both DBC and copper block substrates.

Section 2 Water Spray-Cooling

2.1 Introduction

Thermal management systems for electronics based upon change-of-phase (COP) principles offer several advantages, chief among them being the ability to absorb/release latent heat under quasi-isothermal conditions at the transition temperature [1-7]. Consequently, this phenomenon provides an extremely low, albeit transient, apparent thermal resistance at this temperature, since heat transfer occurs with minimal temperature difference.

Despite this compelling advantage, however, COP thermal management systems have only penetrated a few applications. Part of the reason for the lack of their widespread acceptance is the perceived increase in cost associated with the introduction of a thermal management system that allows either melting and solidification or vaporization and condensation. Another crucial factor is the perceived increase in uncertainty associated with the system stability during a prolonged service life. As a result, electronics applications with lifetimes in excess of 15 – 20 years require a complete understanding of the physics of degradation of the COP thermal management system. Key to addressing these concerns therefore, is the clear demonstration of the performance benefits of COP thermal management systems at the outset, so that an objective assessment of the tradeoffs associated with their implementation is possible. *This objective provided the primary motivation of the present investigation.*

Previously, much work has been performed in systems exhibiting either solid-liquid and liquid-vapor phase transitions [1-7]. However, for most materials, the latent heat of vaporization is significantly higher than the latent heat of fusion [8]. Consequently, liquid/vapor phase transitions were the primary focus of the present investigation. However, as will be described, one ancillary outcome was that superior performance with water-spray cooling is possible even without the necessity of executing the liquid-vapor phase transformation.

One application that requires a demanding combination of electrical performance and thermal management includes adjustable-speed motor drives, e.g., Fig. 16 [9]. Systems capable of controlling power of up to 500 kW are common, with associated high voltage and currents coupled with extreme temperature environments. Here, thermal management is dominated by simple solid-state conduction/air convection systems with commensurate thermal management performance. However, owing to the anticipated performance benefit associated with water-spray cooling, the present investigation was undertaken: namely, *to demonstrate the feasibility and performance characteristics of a water-spray cooling approach to thermal management of high-voltage, high power electronics within a 15-hp motor drive application.*

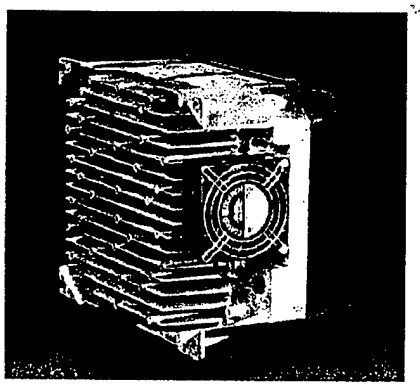


Fig. 16. A typical 5 kW motor drive produced by Rockwell Automation. Such variable-speed motor drives typically exhibit efficiencies on the order of 90 – 95%.

2.2 Results and Discussion

2.2.1 Approach

A water-spray experimental facility suitable for implementation with a 15-hp variable-speed motor drive was developed, comprising a nozzle array, water delivery and recovery system and associated enclosures. The drive module electronics were prepared by removing the protective silicone gel from a commercial 3-phase IGBT power module (eupec BSM 50 GD 120 DN2) and coating the surfaces of the exposed devices and interconnections with a 25 micron Parylene coating through a vapor-phase process. Previous experiments and analysis have established the suitability of this coating in this thickness as a layer with the required dielectric breakdown potential. The nozzle array comprised a square grid of 125-micron diameter holes within a unit cell of 3-mm dimension. This system was connected to a pump (Clarke and Assoc., Model # MGC4-MG209XPC17), filter and flowmeter system capable of supplying 0 – 1 gpm of water operated under controlled, open-loop control. A schematic of this system is shown in Fig. 17, and a photograph of the water-spray nozzle array during operation in Fig. 18.

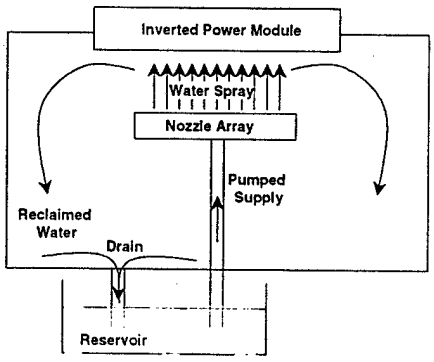


Fig. 17. Schematic of the water-spray facility.

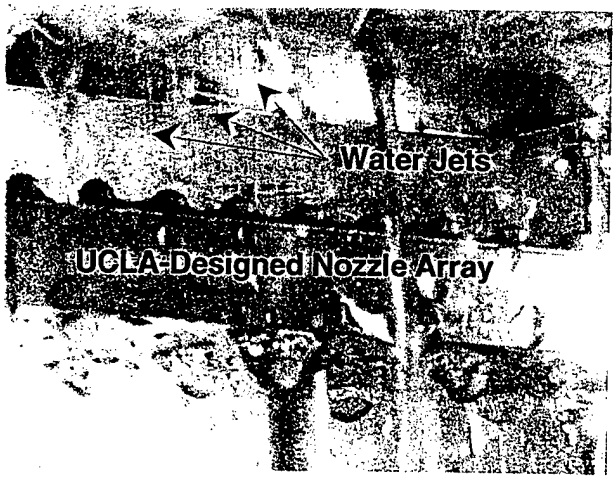


Fig. 18. Photograph of the water-spray nozzle array during operation, as described below.

The AC motor drive system is shown in Figs. 19 – 22, and comprises two primary components – the solid-state drive electronics (Figs. 19, 21, 22) and the AC / DC motor dynamometer (Fig. 20). The implementation of the IGBT module within the system utilizing a conventional air or liquid cooled heatsink is illustrated in Fig. 19, and in the present water-spray cooled facility in Figs. 21 and 22.

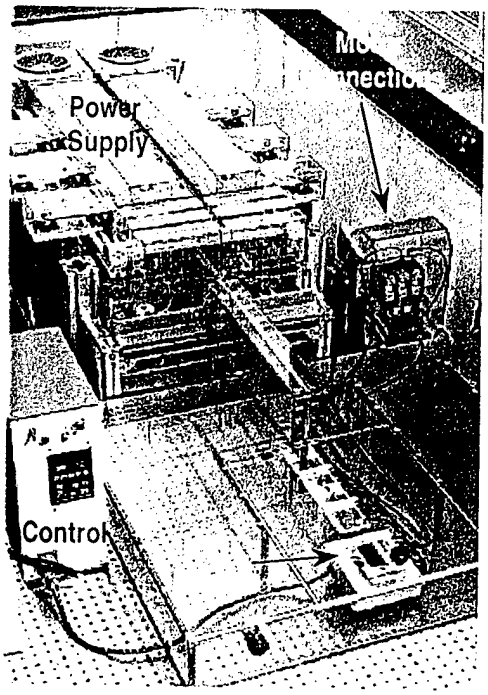


Fig. 19. Photograph of the RSC frameless drive motor drive test facility showing the solid-state drive electronics. An IGBT module is shown attached to a convectively cooled extruded aluminum heatsink.

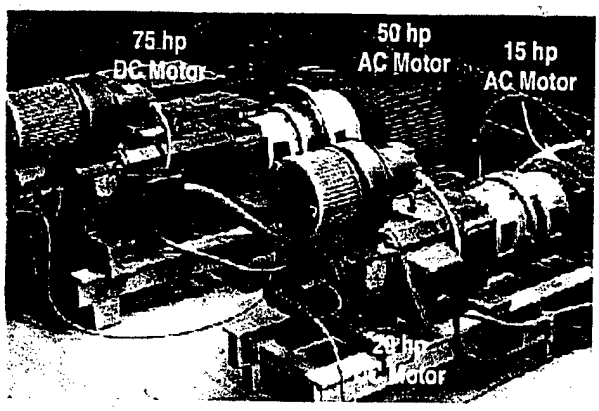


Fig. 20. Photograph of the RSC frameless drive motor drive test facility showing the AC and DC motors comprising the dynamometer.

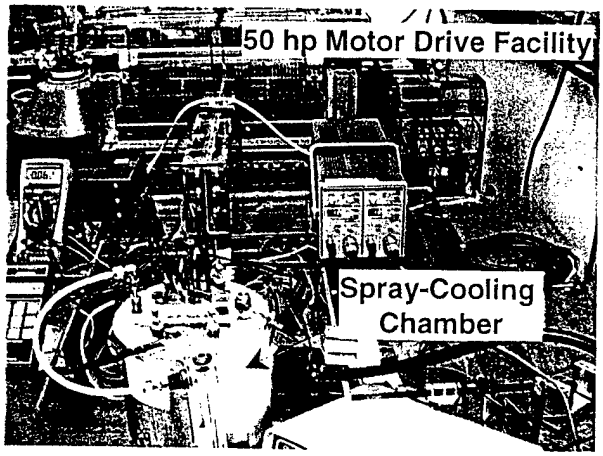


Fig. 21. Photograph of the RSC frameless drive motor drive test facility showing the implemented water-spray cooled experimental apparatus.

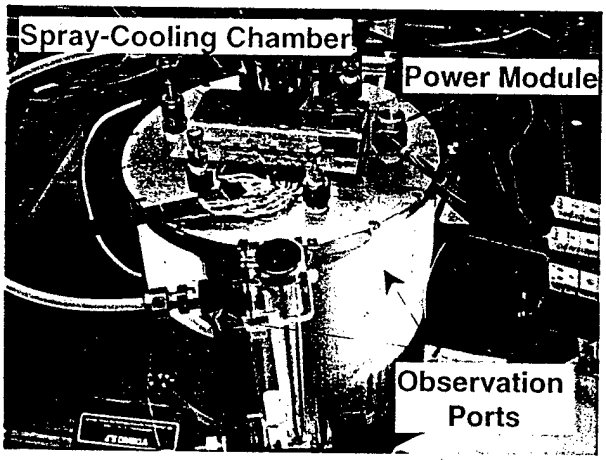


Fig. 22. A close-up photograph of the spray-cooling chamber shown in Fig. 7. Here, the rear of the IGBT power module is clearly visible, as are the windowed observation ports.

Experiments were performed within the three-phase AC motor drive experimental facility described above, with controlled power systematically varied between 0 - 18 hp (13.3 kW). RMS line voltages of up to 325 VAC were utilized with a frequency of 60 Hz for the experiments.

2.2.2 Results

The results of the experimental measurements are summarized in Fig. 23, where a plot of the junction to case temperature increase, ΔT_{jc}, is plotted against dissipated power density within the devices. For the case of the control modules with single IGBTs and single diodes (cf. Fig. 2) the case temperature refers to the temperature at the underside of the DBC substrate. For the case of the water-cooled modules, however, the "case" refers to the temperature of the impinging water. In all instances, a nearly linear increase in ΔT_{jc} was observed with increasing power density, corresponding to a constant thermal resistance for this range of experimental conditions. Also shown on Fig. 23 is the range of typical thermal resistances for commercial motor drives.

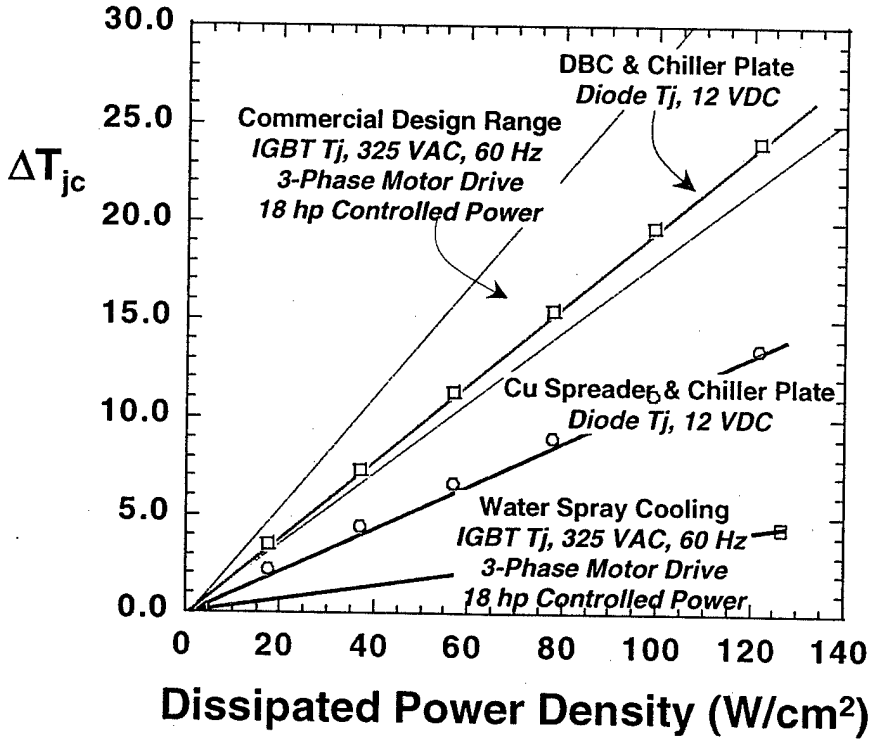


Fig. 23. Experimental results for the thermal performance characterization of the water spray-cooling approach as compared to the baseline control specimens. Also shown, as the shaded region is the typical design range for commercial adjustable speed motor drives. Note the substantially lower temperature increase for the water-spray cooling approach as compared to the others.

For the spray-cooled module, based on a temperature increase of 4.5°C and an estimated power dissipation of 670W within the power module at the maximum controlled power of 13.3 kW, the thermal resistance of the module is 0.007 K/W. Translating this into a thermal resistance per IGBT, based upon 6 IGBTs per module and an estimated 80% power loss within the IGBTs as compared to the diodes, an IGBT chip-to-"case" thermal resistance of 0.05 K/W is obtained. This is approximately seven times lower than the handbook value for the module subject to solid-state conduction coupled to air-cooled convection (0.35 K/W chip to case). *This result clearly establishes the advantage of the water spray-cooling approach.*

Finally, an experiment was performed to elucidate the effect of the flow rate of the water (Fig. 24). As expected, the temperature increase exhibited a nominally inverse relationship with flow rate, although this requires additional studies.

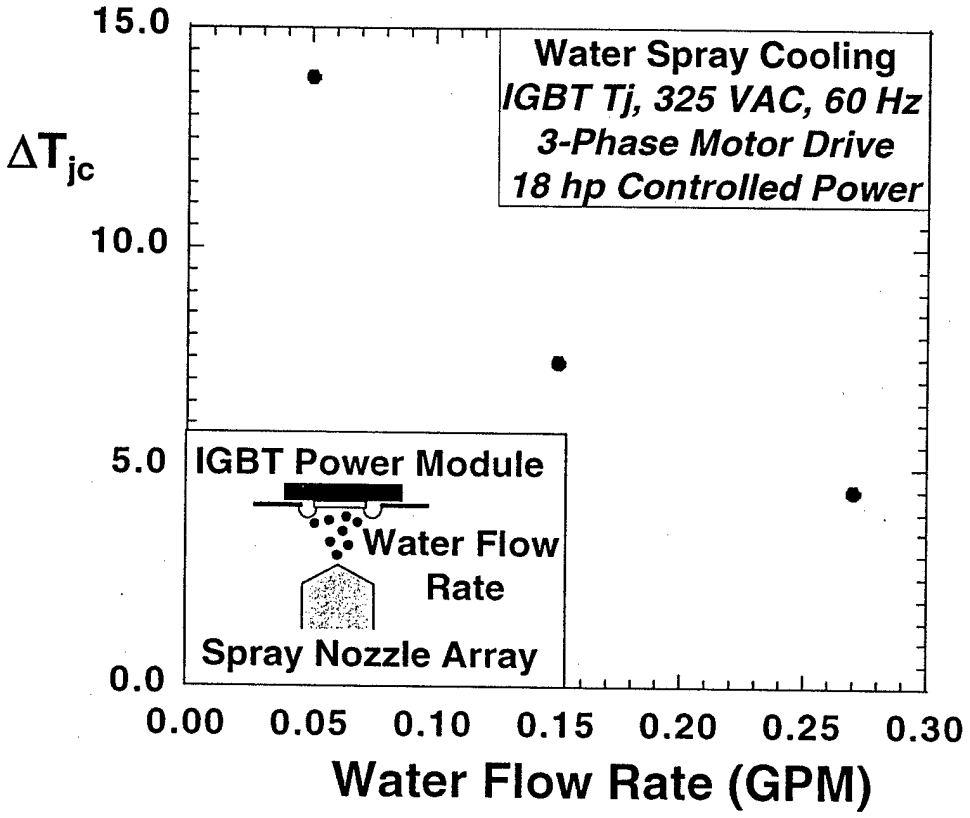


Fig. 24. Experimental results showing the decrease in junction-to-case thermal resistance of the water-spray cooling technique vs. water flow rate.

2.3 Analysis

By performing a simple, physics-based analysis incorporating the mass flow rate of the spraying water, its heat capacity and the power dissipation in the module, a predicted increase in temperature of the water of 8° C is achieved for a dissipated power density of 120 W/cm^2. Although the measured junction temperature increase as compared to the water in the reservoir is only 4.5° C, this discrepancy is associated with external cooling of the water through a refrigerated external cooling system. A secondary source of heat loss is through the uninsulated rear of the module, however, based upon its measured temperature, an estimate of the heat lost through natural convection is only on the order of 1 W.

2.3 Discussion

The predicted junction-to-case temperature increases for the water spray-cooling AC motor drive demonstration and the DBC and copper-block modules are summarized in Table 2. Also shown are the experimentally measured results – *note the drastically reduced junction temperature for the water-spray approach.* Furthermore, the good agreement between the predictions and the measured results for the control modules confirms the significance of the heat-spreading phenomenon in reducing the thermal resistance of the copper-block module as compared to the DBC module as well as the modeling approach.

Table 2. Comparison of Predicted and Measured ΔT_{jc}

	ΔT_{jc} at 120 W/cm^2 (°C)	
	Predicted (Analytical)	*Measured*
DBC module	24.1	24.6
Cu-block module	13.6	13.6
Water-spray cooling	8	4.5

Based on these results, the following conclusions may be drawn (Section 2):

1) The dramatically reduced junction temperature and thermal resistance for the water spray-cooled module compellingly demonstrates the suitability of the approach.
2) The present successful integration of water spray-cooling directly on the parylene coated, high-voltage (325 VAC) AC motor drive electronics is the first of its kind, to our knowledge.
3) The thermal resistance of the copper-block module is less than that of the DBC module, and results from major differences in geometry-controlled heat-spreading.
4) The thermal resistance of both the copper-block and DBC modules is essentially invariant with dissipated power/temperature over this range of conditions.

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